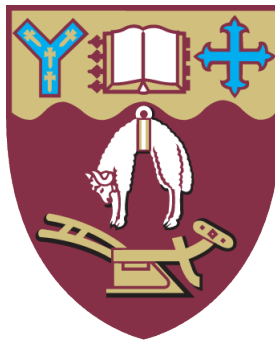


SOFTWARE DEFINED RADIO FOR MARITIME COLLISION AVOIDANCE APPLICATIONS

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ABSTRACT

The design and development of a software defined radio (SDR) receiver prototype has been completed. The goal is to replace the existing automatic identification system (AIS) manufactured by Vesper Marine with a software driven system that reduces costs and provides a high degree of reconfigurability. One of the key concepts of the SDR is the consideration of directly digitizing the radio frequency (RF) signal using subsampling. This idea arises from the ambition to implement an analog-to-digital converter (ADC) as close to the antenna interface as practically possible. Thus, majority of the RF processing is encapsulated within in the digital domain. Evaluation of a frequency planning strategy that utilizes a combination of subsampling and oversampling will illustrate how the maritime bandwidth is aliased to a lower frequency. An analog front-end (AFE) board was constructed to implement the frequency planning strategy so that the digitized bandwidth can be streamed into a field programmable gate array (FPGA) for real-time processing. Research is shown on digital front-end (DFE) techniques that condition the digitized maritime signal for baseband processing. The process of a digital down converter (DDC) is conducted by an FPGA, which acquired the in-phase and quadrature signals. By implementing a digital signal processor (DSP) for baseband processing, demodulation on an AIS test signal is evaluated. The SDR prototype achieved a receiver sensitivity of -113dBm, outperforming the required sensitivity of -107dBm specified in the International Electrotechnical Commission (IEC) 62287-1 standard for AIS applications [1].

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ABBREVIATIONS

ADC	Analog-to-Digital Converter.
AFE	Analog Front-End.
AGC	Automatic Gain Controller.
AIS	Automatic Identification System.
BOM	Bill of Materials.
CCES	Cross Core Embedded Studio.
CSTDMA	Carrier-Sense Time Division Multiple Access.
DFE	Digital Front-End.
DMA	Direct Memory Access.
DSC	Digital Selective Calling.
ENOB	Effective Number of Bits.
FDA	Filter Design and Analysis.
IC	Integrated Circuit.
IEC	International Electrotechnical Commission.
IF	Intermediate Frequency.
ISR	Interrupt Service Routine.
ITU	International Telecommunication Union.
LO	Local Oscillator.
LSB	Least Significant Bit.
MSB	Most Significant Bit.
NF	Noise Figure.
NMEA	National Marine Electronics Association.
NRZI	Non-Return to Zero Inverted.
PER	Packet Error Rate.
PLL	Phase-Lock Loop.

PPI	Parallel Port Interface.
PSD	Power Spectral Density.
RF	Radio Frequency.
SFDR	Spurious-free Dynamic Range.
SINAD	Signal-to-Noise and Distortion.
SNR	Signal-to-Noise Ratio.
SNRFS	Signal -to-noise Radio Full Scale.
SOLAS	Safety Of Life At Sea.
SOTDMA	Self-Organised Time Division Multiple Access.
SPORT	Serial Port.
SDR	Software Defined Radio.
UHF	Ultra High Frequency.
VDM	VHF Data-link Message.
VDO	VHF Data-link Own vessel message.
VGA	Variable Gain Amplifier.
VHF	Very High Frequency.
VTs	Vessel Traffic Service.
WRC	Wireless Research Centre.

Chapter 1

INTRODUCTION

This chapter describes the motivation behind this research by presenting the problem statement and focus. A brief introduction to software defined radio (SDR) architecture provides an outlook on the ideas for this project. This is then followed by the research objectives. At the end of this chapter an outline for the remainder of the thesis is provided.

The idea behind developing SDR technology is to provide a solution for high speed signal processing requirements that allow software driven flexibility. SDR supports the ability to apply modifications to baseband subsystems, offering redesigns and development for different applications via software [2–4]. Through the use of programmable devices, a digital hardware platform can be constructed to execute the software designs. However, at the antenna interface the incoming radio signals is analog. Therefore, the radio cannot not be entirely characterized by software. An analog front-end (AFE) must be integrated to condition the radio frequency (RF) signal before it becomes digitized [2]. Hence the name software *defined* radio. The dream of a “pure” software radio began with the appearance of discrete logic components, microprocessors and microcontrollers, which replaced analog components. For many radio receivers, digital signal processor (DSP) devices have permitted analog signals to be processed digitally, dramatically reducing, or even eliminating active and passive electronic circuitry.

This project aims at designing and developing a SDR prototype using modern technologies. Investigation and implementation of components such as ADCs, DSPs and field programmable gate arrays (FPGA) that provide the software radio functionally will be detailed. This project goes beyond traditional analog RF approaches, and looks towards gaining a step closer to designing a radio fully characterized by software. One of the key focuses in this research is to exploit direct digitization techniques at RF by performing subsampling, with the objective being: to

lower costs, reduce board space and add flexibility by digitizing the very high frequency (VHF) marine band as close to the antenna interface as possible. From this, digital signal processing algorithms and RF down-conversion techniques will be investigated and applied as a solution for Vesper Marine's collision avoidance safety equipment.

1.1 VESPER MARINE

Vesper Marine are manufacturers of innovative marine safety equipment that utilize an automatic identification system (AIS). Their AIS products provide a tracking system used for vessel traffic services (VTS) in maritime collision avoidance applications [5]. Vesper Marine are based in Auckland, New Zealand. The team are a small group of specialized product engineers and customer service technicians, who are supported by a worldwide distribution network of marine electronic experts [5].

The existing Vesper Marine products are based on a AIS engine circuit board known as Mimosa. Traditional superheterodyne receiver techniques are implemented on the Mimosa to support the dual channel VHF transmit and receive paths. The modulated and demodulated audio signals are converted to a digital format, known as NMEA 0183, using a specialised co-processor from CML Microcircuits, enabling data acquisition from a microprocessor. The AIS Engine performs very well. However, there are a number of major disadvantages that must be resolved.

1.2 PROBLEM STATEMENT AND FOCUS

With the rapid growth in discrete logic components, semiconductor manufacturers are migrating away from the VHF band to the more market dominant ultra high frequency (UHF) band. As a result, component obsolescences on parts for many VHF applications are becoming a recurring issue. When products have to be internationally certified to rigorous standards, a part swap will require re-certification, and is thus exhausting on engineering and production resources. This trend is becoming more and more common with the advancements in technology.

Currently, the Mimosa board has a reliance on the CMX7032, provided by CML Microcircuits [6]. Dependence on single source IC chip's can be problematic in the foreseeable future. Traditionally, communication systems require specialized hardware, such as IC's to implement

signal processing. For efficient design, the make up of these systems conduct specific functions that only acquire the necessary outputs. As a result, redesigns to the systems architecture can be very complicated.

Another limiting factor used on the Mimosa is its superheterodyne receiver signal chain. Over the last century the superheterodyne receiver has been a common architecture in radio systems. The popularity of this receiver type comes from its great performance regarding selectivity and sensitivity. The advantage of the superheterodyne receiver lies in the ability to convert incoming RF signals down to an intermediate frequency (IF). The use of an IF stage gives the receiver great channel selectivity performance because it relaxes the complexity of filters and amplifiers [7]. However, the capability to convert to lower frequencies also contribute to certain disadvantages. The number of components required to carry out the conversion to IF results in larger board space, power consumption and architecture complexity [8]. Acquiring flexibility subsequently becomes a challenging task because the components used at IF are fixed in frequency, typically used for narrowband channels. Therefore, the system is only capable of accessing a small part of the spectrum.

The block diagram displayed in Figure 1.1 is the architecture of the AIS receiver signal chain. Note the number of processing stages the received signal must pass through to preserve the desired information. An IF stage is used on two separate frequency modulated, Gaussian Minimum Shift Keying (FM/GMSK) based receiver channels, both using filters and FM discriminators to preserve and obtain the audio signal respectively. The CMX7032 is used to process the incoming AIS audio signals, providing the TxD output as NMEA 0183 formatted data [9].

The solution proposed is a new SDR platform, which will replace the existing superheterodyne architecture on the Mimosa. The idea is to execute as much signal processing as possible in the digital domain using software. This approach shifts the core signal processing intellectual property (IP) into the software domain, taking away any reliance on single source parts. The design will provide IP sustainability as semiconductor manufacturers in ADC, DSP and FPGA will continue to grow for the foreseeable future. SDR technology not only will simplify manufacturing and production support, it also provides the flexibility to implement different modulation schemes and frequencies without the need for complicating hardware designs. This also gives Vesper Marine the opportunity to provide solutions within different markets.

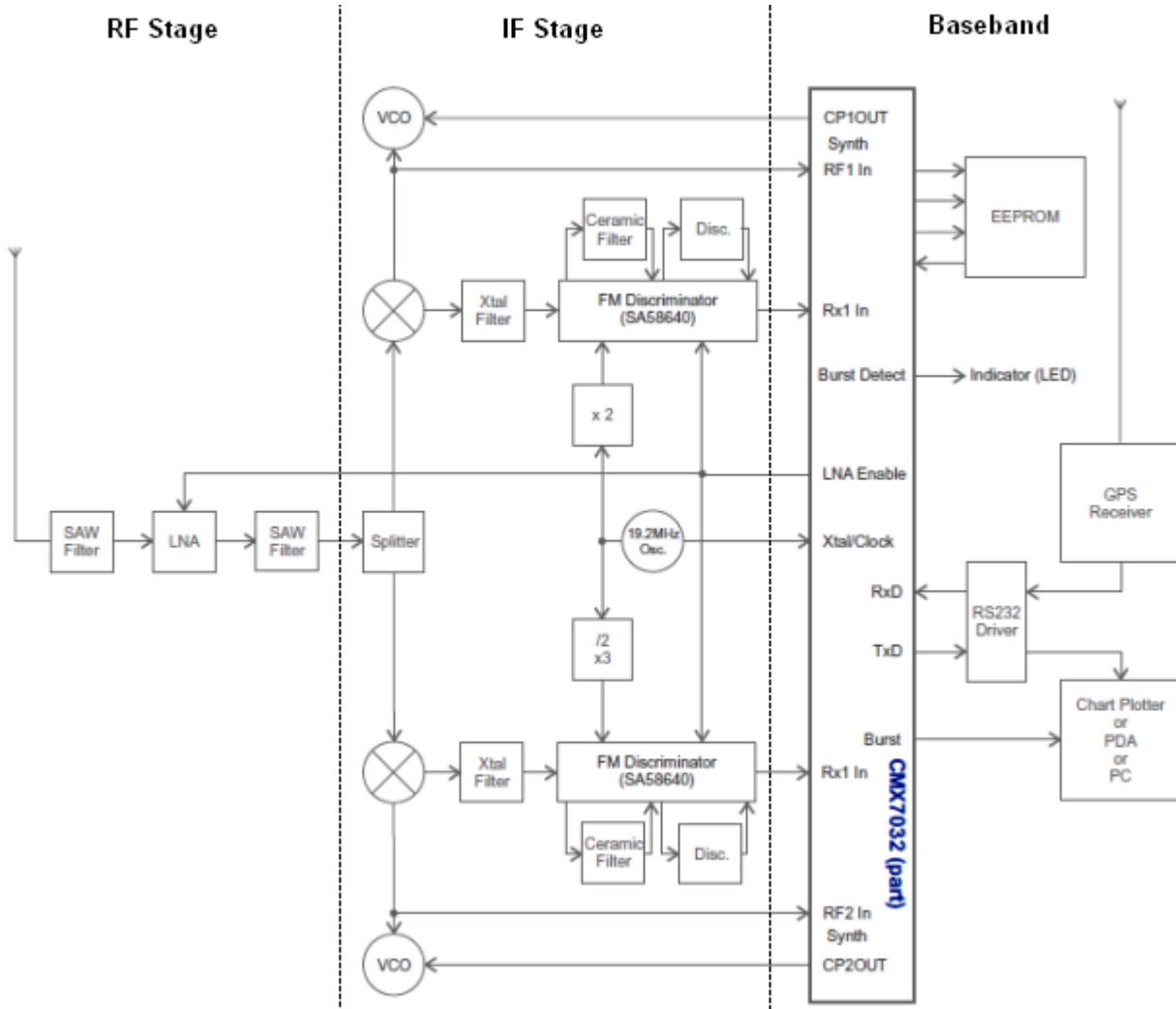


Figure 1.1: Block diagram of the superheterodyne receive-only architecture used for AIS products [9].

1.3 SDR ARCHITECTURE

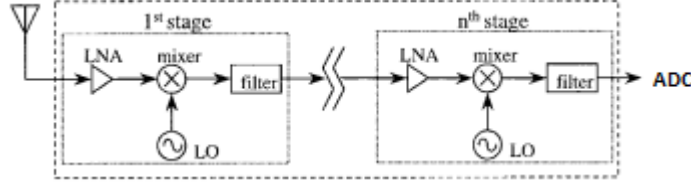
For a communication system to achieve the ideal “pure” software radio, the analog signals at the antenna would be immediately quantized. For current communication standards, this approach imposes requirements on ADC’s beyond the state of the art. The liberation is accomplished through a combination of techniques that includes band-limiting the receivers capacity to listen to air waves. The VHF maritime radio band is located in the spectrum from 156.025MHz to 162.025MHz. Therefore, the system can be fixed on a wideband (6MHz) that contains many different narrowband (25kHz to 50kHz) channels. In today’s wideband ADC technology, quantizing a 6MHz band can be accomplished. However, the SDR under discussion is interested in

quantizing the 6MHz band directly from the VHF maritime bandwidth. To achieve this we must consider SDR design techniques such as sample theory, frequency conversion and digital signal processing. The SDR architecture introduced in this section will describe the methods and technologies that will enable the development of a software-based radio platform. An introduction to AFE signal chains will present the idea of directly digitizing the maritime bandwidth. Digital signal processing techniques will also be introduced that conduct the software algorithms for acquiring the desired channel information. This will follow design considerations for a programmable platform that execute software functionality. The ideas from this section will be referred to throughout this thesis.

1.3.1 Analog Front-End Signal Chain

Traditionally, the front-end signal chain preceding the ADC comprises of a number of stages as shown in Figure 1.2a that mix the RF signal to a manageable IF, relaxing the ADC's throughput [7, 10]. Generally, high resolution ADC's are implemented at lower throughput or sample rates to provide better receiver performance. Whereas, high speed ADC's typically sacrifice resolution for speed. This is one of the principle trade-offs in system designs that require high speed analog-to-digital conversion. In many cases, the ADC defines the systems receiver bandwidth, dynamic range and power consumption. It becomes a very challenging tasks to implement wideband ADC's in software radio design. For example, in digitizing the VHF maritime radio band of 6MHz, a multitude of channels as well as unwanted signals will be received. The ADC is responsible for quantizing all signals safely into the digital domain, no matter how weak or strong. The ADC's capability to digitize a range of different signal levels is quantified by the ADC's dynamic range and resolution. Directly connecting the antenna to the ADC to quantize the VHF signals would result in conflicting requirements: a very high sampling rate, a large bandwidth and a high dynamic range while avoiding intolerable power consumption [11].

To find a solution that avoids these conflicting requirements, an understanding of sample theory must first be obtained. According to Nyquist's Criteria, the ADC must operate at a sample rate, f_s , greater than or equal to twice the highest frequency component of an analog signal, f_a , ($f_s \geq 2f_a$) in order to preserve the original information without aliasing [12]. Further details are presented in Section 2.3. The highest channel frequency in the maritime radio band



(a) A typical superheterodyne receiver, illustrating the IF stages in the receiver signal chain.



(b) The direct digitization receiver, consisting of low-noise amplifier (LNA) and band-pass filter (BPF).

Figure 1.2: An illustration of the superheterodyne and direct digitization receivers [10].

is 162.025MHz. Therefore, the minimum sample rate required to preserve all signals components up to 162.025MHz is $f_s=324.050\text{MHz}$. With present ADC technology, digitizing and processing at sample rates around 324.050MHz is known to be possible. Modern ADC's can digitize in the GHz range [13], and with the growth in FPGA technology the process power required to implement digital signal processing can be matched. However, operating at high speed sample rates comes at the price of high performing technology. For example, the AD9434-370 from Analog Devices has the capability to sample at 370MHz with a resolution of 12-bits [14]. At the cost \$100.00 (USD) per device [15] the AD9434-370 is not suitable for the AIS unit to compete with market demands. Other methods must be devised to achieve a marketable SDR platform. One possible option would be to include a down-conversion stages between the antenna and ADC [16]. Although, this goes against the philosophy of the software radio design.

Figure 1.3 illustrates the spectrum that gets digitized by the ADC with a sample rate, $f_s=324.050\text{MHz}$. To prevent digitizing and aliasing unwanted noise a LPF is used preceding the ADC for anti-aliasing purposes. Following Nyquist's Criteria ($f_s \geq 2f_a$), the signal components from DC to 162.025MHz get successfully digitized. This means that the SDR will have a receiver bandwidth of 162.025MHz. As discussed earlier, we are only interested in the maritime band. Therefore, it makes sense that a SDR should only require a receiver bandwidth of $\geq 6\text{MHz}$. This notion leads to the method of band-pass sampling or subsampling, which derives from Nyquist's Criteria. It implies that the sample rate required to preserve the maritime band is not imposed by the highest signal component ($f_a=162.025\text{MHz}$) but the size of the bandwidth ($\text{BW}=6\text{MHz}$). The new version of the Nyquist Criteria requires a sample rate of $f_s \geq 2\text{BW}$.

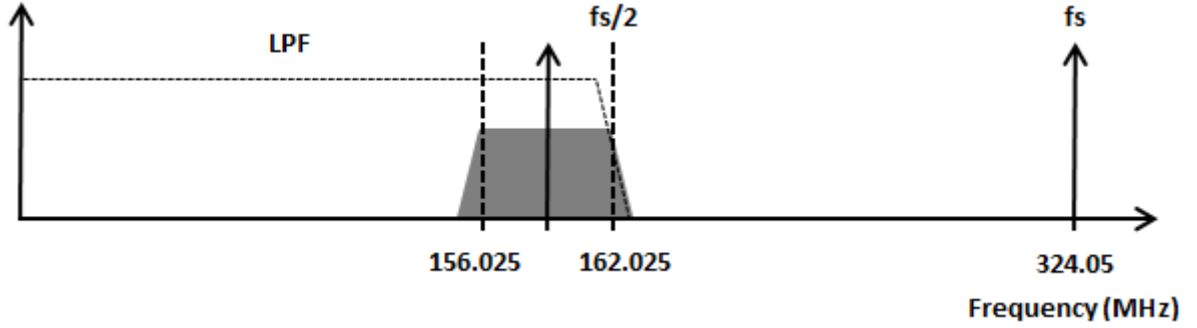


Figure 1.3: The spectrum of the maritime band following the Nyquist Criteria ($f_s \geq 2f_a$) sampled at a rate, $f_s=324.050\text{MHz}$.

Therefore, we can preserve all the signal components within the maritime band by applying a sample rate of $f_s \geq 12\text{MHz}$.

Subsampling intentionally aliases the bandwidth of interest, creating images viewed as frequency translated versions of the desired information, instead of unwanted by-products. Figure 1.4 demonstrates the images (aliased components) after digitizing the maritime band using subsampling. Note that the anti-aliasing filter for subsampling requires a band-pass filter (BPF) preceding the ADC. The approach of subsampling also has the effect of down-converting the desired bandwidth to lower frequency bands. Figure 1.4 shows that the maritime bandwidth is now located between DC and $f_s/2$. Images of the maritime band are created about each sample frequency harmonic. The method of subsampling takes advantage of the aliased components. From Figure 1.4 we can see that the sample rate can be reduce to $f_s \geq 12\text{MHz}$ to capture the 6MHz maritime band. This significantly reduces the speed requirement of the ADC, allowing

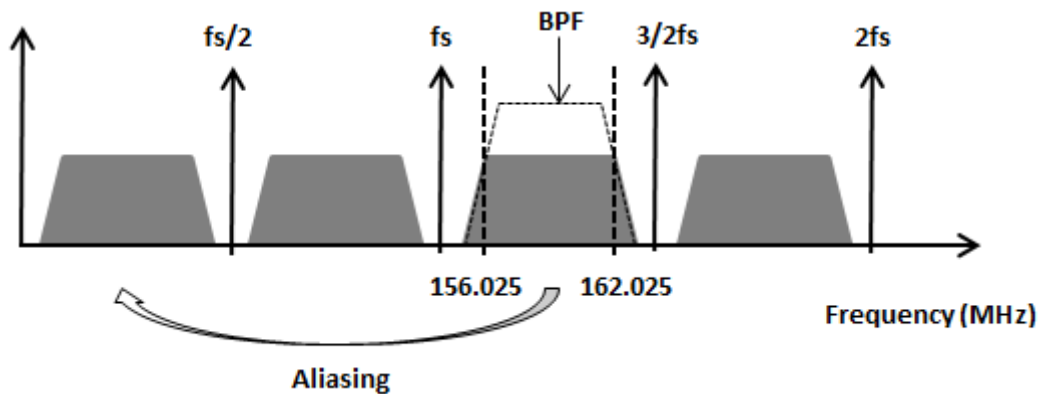


Figure 1.4: An illustration of the aliased maritime band throughout the spectrum as a result of implementing subsampling.

the use of a more high resolution and inexpensive device. With this in mind, a direct digitization receiver architecture that utilizing subsampling is a very attractive method and will be explored throughout this thesis.

Following the method of moving the ADC as close to the antenna as possible [2, 8, 10], the minimal set of components used in the front-end is shown in Figure 1.2b. The direct digitization method band-limits the incoming signal to be digitized, as shown in Figure 1.4, which is accomplished through the use of a BPF [10]. The incoming signals at the ADC input are also condition through an amplifier stage, typically through the use of Low Noise Amplifier's (LNA), which provide the ADC with a suitable input levels for the analog-to-digital conversion. The minimal processing required in the front-end makes the direct digitization architecture an attractive approach for the SDR platform. However, the receiver relies heavily on the ADC' performance. This project will provide research in to ADC technology, and aim to implement the direct digitalization technique that utilizes subsampling to capture the maritime band. Performance will be analysed and compared to the International Electrotechnical Commission (IEC) 62287-1 standards for AIS receivers [1].

1.3.2 Digital Front-End Signal Chain

Receiver systems are generally designed to select and process desired signals to acquire useful information. With the intention to minimize the signal processing stages within the AFE, it is in the digital front-end (DFE) signal chain where the desired signal is selected and converted to baseband for data acquisition. Once the maritime bandwidth has successfully entered the digital domain, the programmable features of the SDR come to fruition. The digitized maritime band of frequencies will be aliased to a digital IF band, This is shown as the aliased component between DC and $f_s/2$ in Figure 1.4. The functions that follow the ADC are typically in the form of channel selection, frequency conversion, filtering and sample rate conversion [17]. These functions in the DFE signal chain form the digital down converter (DDC), that obtains the in-phase (I) and quadrature (Q) components. An illustration of the DFE is presented in Figure 1.5.

From Section 1.3.1, it is known that the AFE signal chain captures a bandwidth of 6MHz, consisting of multiple digitized channels that are made available for the programmable device

for processing. It is likely that unwanted signals will also lie within the digitized bandwidth, considering it spans 6MHz. Therefore, the DFE must provide processing stages to condition the desired channel leading up to basband processing. To convert the wanted channel signal to baseband a down-conversion stage from digital IF is used, this typically come in the form of mixing a digitally generated signal with the desired channel. The beauty of implementing the IF stage within the digital domain rather than the analog is that the flexibility of channel selection and/or number of channels to execute is entirely defined by the software. The functions of the DDC structure, as shown in the blown up box in Figure 1.5 can be described by the two following methods:

- Channelization,
 - the process of down-converting the channel-of-interest from digital IF to baseband, and
 - filtering, removing out-of-band channel interferers and quantization noise.
- Sample rate conversion,
 - typically in the form of decimation to decrease the sample rate of the channel-of-interest.

It should be noted that the order of the processing stages shown in the DDC structure from Figure 1.5 is not a requirement. The process of channelization is accomplished by locally generating a digital sine wave from a local oscillator (LO) that is tuned to the frequency of the channel of interest. By using two generated waveforms with a 90° phase shift difference, it is possible to acquire the I and Q components at baseband [18]. The I and Q components provide the information necessary to demodulated the signal. Once the channel has been selected, the spectrum outside the channel bandwidth becomes redundant. Therefore, the sample rate required to capture the wideband signal is no longer essential. Hence, the DDC decimates (down-samples) the channel to a lower data rate for baseband processing. The I and Q component are then filtered at the lower data rate to complete the I and Q demodulation process.

The process of channelization and sample rate conversion is typically executed at high processing speeds, corresponding to the wideband signal. For AIS, the sample rate required will be $\geq 12\text{MHz}$ as discussed in Section 1.3.1. As mentioned earlier processing at rates of $\geq 12\text{MHz}$ applies a heavy processor load, particularly for commercial processors. Devices with programmable feature that can tolerate these types of processing speeds typically come in the form of hardware

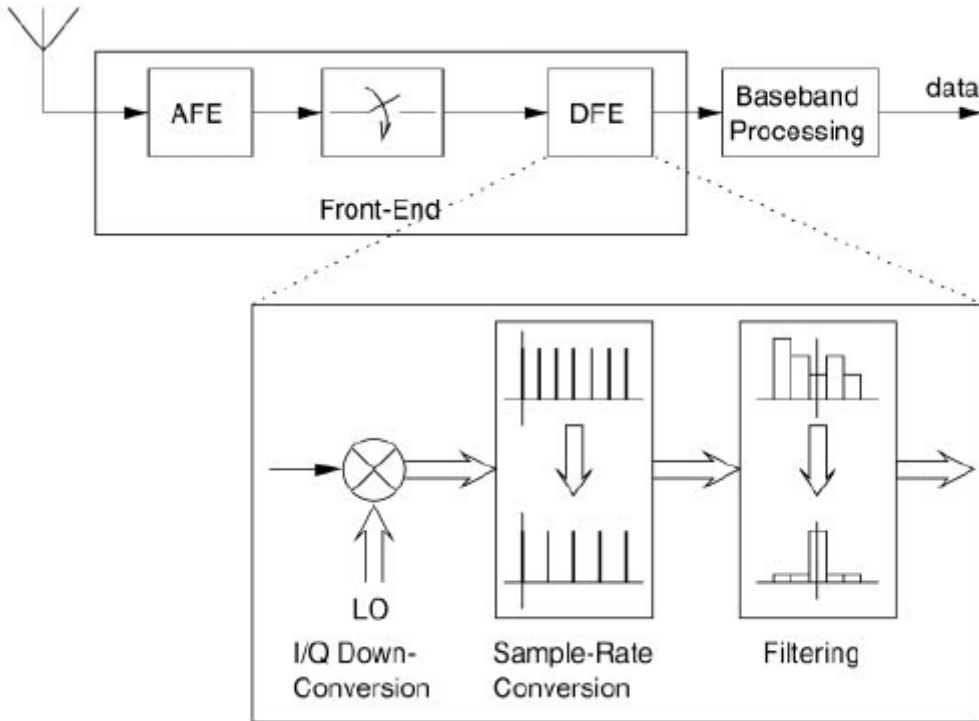


Figure 1.5: Digital front-end of a SDR signal chain [2].

configurable devices such as an FPGA. However, the advantage in implementing the DDC is that the data rate is decimated to a lower sample rate, which is used to represent the I and Q components at baseband. The I and Q data obtained from the channel will generally be at speeds of 50kHz to 100kHz for narrowband signals such as AIS channels. With this in mind, the possibility of implementing a device such as a DSP at baseband is very plausible.

1.3.3 Baseband Processing

The baseband processing stage imparts the first level of channel demodulation, acquiring the message signal and data that is modulated on the carrier waveform. The complexity of the baseband algorithms to recover the information depends on the channel's bandwidth and modulation scheme [19]. For AIS applications, the modulation used is FM/GMSK because of its robustness, discrimination characteristic, bandwidth efficiency and its application in mobile digital communications [20]. From Figure 1.1, the receiver path on the Mimosa board consists of FM discriminators, which are fed the channel of interest at IF to recover the AIS audio signal through FM demodulation. This presents the baseband signal that allows data acquisition by

the CMX7032. The information produced by the CMX chip is in the form of an AIS message, that known as VHF data-link message (VDM). VDM's provide a sentence that encapsulates meaningful AIS information that is broadcast by AIS users. Decoding the VDM sentence provides the identification information that is used by an application processor to deliver the AIS information via a display such as a chart plotter.

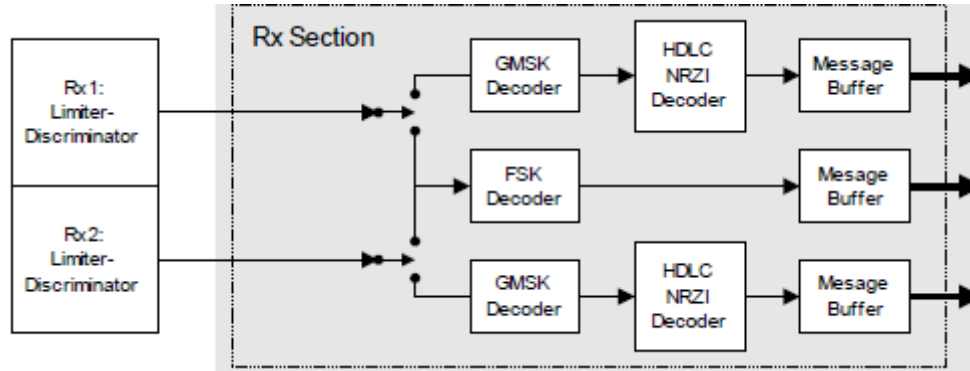


Figure 1.6: Diagram of the receiver section within the CMX 7032 chip [6].

In Section 1.3.2, the DFE signal chain provides the I and Q components necessary to execute demodulation on the FM/GMSK channel at baseband. Within the SDR's programmable platform the AIS audio signal can be produced by a discrete FM demodulator. The programmable platform must also have the capability to encapsulate the receiver section of the CMX7032 as shown in Figure 1.6, used to obtain the VDM information. It is not in this projects scope to develop the software that executes the functionalities of the CMX's baseband processing. However, is we know that these functions are digitally conducted in the CMX. Therefore, it is possible to develop and transitions of it's function can achieved in a DSP.

The research from this project will investigate and develop a software-based platform that achieves the AIS audio signal within the SDR by implementing FM demodulation. By acquiring the AIS audio signal we can test receiver performance parameters such as sensitivity and adjacent channel sensitivity, and compare the results to IEC 62287-1 receiver standards. Further investigation will also be done on displaying and recovering the VDM sentence. To show that the SDR receiver signal chain can in fact accomplish the AIS information, the FM demodulated audio signal from the SDR can be fed into the CMX7032 on the Mimosa as a proof of concept, displaying the entire receiver path from RF to the AIS information.

1.3.4 Programmable Platform

Development of a real-time software radio platform can be built using a variety of digital hardware. Typically involving computer-aided design of the logic resources and mathematical arithmetic. One of the key objectives in developing a software radio platform is to attain a high level of reconfigurability. Employing programmable hardware provides the basis to execute reconfigurable designs. Performance may be quantified by power consumption, relative costs, and computational capability metrics [21]. The performance metrics must be balanced with each other in the overall design. Defining broad fundamental performance metrics relative to the systems application is one of the principle challenges in designing a programmable platform. Shifting the majority of signal processing in to the digital domain puts much of the processing load onto the programmable device(s). Particularly when we are considering the using high sample rates to capture signals at the VHF maritime band, the throughput of data can be strenuous on the programmable platform, and may require undesirable costs and power consumption.

For programmability and fast time-to-design the DSP excels, supporting programming in high level languages such as C. DSPs have a microprocessor-based architecture that provide a high degree of flexibility in both software and hardware. However, today's DSPs alone cannot handle processing complex algorithms at high speeds required for the maritime bandwidth without consuming a reasonable amount of power. FPGAs however, implement hardware reconfigurations, making it possible to execute complex algorithms at high speed. Software tools for FPGAs, allows designers to parametrise the hardware-layer configuration through its logic resources. The cost of logic resources required to fulfil digital signal processing functions typically result in high priced devices. Overall, these two types of programmable hardware devices tailor to a design that presents tradeoffs in flexibility, processing speed, power consumption and cost [21]. It becomes a difficult task to design a programmable platform that satisfies these tradeoffs.

The digital hardware used in a software radio platform is ultimately dictated by the constraints of the application. The hardware must be scalable to cater to the requirements of the AIS functions. As mentioned in Section 1.3.1 the maritime bandwidth for AIS requires a minimum sample rate of 12MHz to achieve successful digitization. The amount of processing power necessary to perform algorithms on this information in real-time is one of the underlying design constraints. In developing commercial products one must bear in mind that the biggest selling

points in a commercial product is cost. This shifts focus on implementing and developing optimum signal processing techniques and algorithms that minimise process loads, relaxing the constraints presented by the AIS characteristic.

In Section 1.3.2, the implementation of the DDC showed that the high speed sample rate ($f_s \geq 12\text{MHz}$) requirement of the ADC can be decimated to a lower rate. The AIS baseband signal has a bandwidth of 25kHz, therefore, a sample rate of approximately 50kHz to 100KHz will be required. It is possible to partition the process speeds between a FPGA and DSP, with the idea being to dedicate the FPGA as the DFE that produces the I and Q components at a decimated sample rate. The DDC functions show little complexity so costs can be reduced. By implementing a DSP, the baseband algorithms for AIS signal can be implemented using at a lower process speed, making it less power hungry. Moreover, encapsulating the CMX's functions with software is less complicated within a processor type structure like the DSP. Research into the implementation of a FPGA and DSP that completes the digital receiver signal chain will be investigated. Evaluation boards will be used to implement the processes that acquire the AIS information in real-time.

1.4 RESEARCH OBJECTIVE

SDR is a technology waiting for an application. This project presents research in software radio design techniques that can be applied to maritime AIS products. Specified standards under the IEC regulations for maritime public safety [1] must be considered and achieved. SDR technology has many benefits, however, the problem with software radio platforms is the tradeoffs between the required sample rates, processing power and costs to achieve a practical system. The existing receiver architecture on the Mimosa provides a template for the functionality of the system. The challenge for this project is to identify solutions to execute and improve the current AIS designs using a programmable platform. The functional goals are to receive and perform FM demodulation on AIS signals, outputting an audio signal containing the AIS information. Engulfing the CMX7032 functionality is outside the scope of this project. Instead, the focus is on developing a prototype that can perform the functionalities of a SDR receiver that meets AIS performance requirements by implementing direct digitization using subsampling. A SDR prototype developed from this project will provide the platform to execute the AIS baseband processing of the

CMX7032 by further developing the software in the DSP.

Moving towards the philosophy of a software radio, this research investigates the direct digitization architecture. The approach of intentionally aliasing the maritime bandwidth through the using of subsampling shows potential to reduce the number analog processing stages in the AFE, and thereby minimises costs and board space. This research will investigate a frequency planning strategy that combines subsampling and oversampling to successfully alias and capture the VHF maritime bandwidth. The analysis will lead to the investigation of DDC structures that can provide practical methods, which can be exploited in an FPGA.

The SDR design will be compared to IEC standards for AIS receivers to provide performance criteria. In all public safety radio equipment achieving the required receivers sensitivity is one of the primary goals. The SDR platform will target a receiver sensitivity of -7dBm to -113dBm [1]. To accomplish this, the AFE signal chain must have the capability to provide an input signal to the ADC that maintains the receivers SNR for successful digitization. This will lead to the development of a front-end prototype board that will incorporate filtering and amplifier techniques that condition the incoming signal. It is known that the receiver design relies heavily on the ADC. Research gathered on the ADCs available in today's current market will provide a basis for the development of the direct digitization receiver. This research will provide information on the important design parameters to target, and the essential methods for hardware design.

The principal goal of this project is to implement methods that accomplish SDR characteristics into to a prototype. This will follow the development of hardware and software directed at AIS functionality. To formulate a methodology of constructing the prototype, research into digital hardware must also be completed. This search centres on ADCs, FPGAs and DSPs. For fast time-to-design, evaluation hardware will be used to implement techniques using software environments. Utilising evaluation boards for respective ADC, FPGA and DSP devices, the aim is to investigate the following:

- ADC evaluation board,

Using AIS signals, investigate direct digitization using subsampling to alias the maritime bandwidth down to a digital IF band. Evaluate different sample rates that digitize wide-band signals, whilst providing efficient dynamic range.

- FPGA evaluation board,

Capture and process the digitized maritime band. The software developed will target the digital IF band to implement DDC processing, obtaining the channel-of-interest at base-band in it's I and Q components.

- DSP evaluation board,

Execute discrete FM demodulation on the channel-of-interest to accomplish the AIS audio signal.

Implementing SDR techniques using evaluation boards, will follow testing and comparisons to AIS standards. Throughout the process of implementation, algorithms will be developed to condition the digital signal and extract audio information. This project will look into methods that can potentially reduce hardware resources so that inexpensive, low power programmable devices can be used. From this, a prototype SDR platform will be designed and constructed that can receiver and recover AIS information.

1.5 THESIS OUTLINE

In Chapter 2, background on some of the key areas on SDR design are detailed. Section 2.1 describes the functions of AIS and the receiver standards required for AIS products. There is also a functional description of the Mimosa board used in the current AIS products from Vesper. Section 2.2 describes different RF receiver architectures and compares, where possible, the advantages and disadvantages of each receiver. The following subsection gives the digitization methods of a SDR receiver, focusing on subsampling and oversampling techniques. Some of the important performance measures for digital receivers are given in Section 2.4. The digital signal processing involved with DDC is described in Section 2.5. A discrete FM demodulation method for baseband processing is presented in Section 2.6.

Implementation of the AFE and the design techniques used, are described in Chapter 3. In Section 3.1, implementation of subsampling the maritime bandwidth is shown, also discussed, is the benefits of applying oversampling to a frequency planing strategy. The analysis follows the selection of an ADC for the SDR platform. Section 3.2 implements and evaluates the ADC that subsamples the maritime bandwidth through the use of an evaluation board. This presents FFT

results on the quantized signal. To develop the AFE preceding the ADC, Section 3.3 presents the structure of the amplifier and filter designs. The final build of the AFE prototype board is shown in Section 3.4, where results are gathered on the direct digitization structure.

Chapter 4 details the implementation of the DFE signal chain. Section 4.1 illustrates the design of the I and Q demodulator and the decimation stage for the DDC structure. The hardware requirements are discussed in Section 4.2, that provide the designs of the complete SDR receiver signal chain. Finally, in Section 4.3, the software implementation is described that completes the DDC and FM demodulation processes.

Results of the complete SDR prototype are given in Chapter 5. The structure of the SDR under testing conditions is shown. The test methods and results are compared, where possible, to the IEC 62287-1 receiver standards. This follows a comparison in costs between the existing architecture used on the Mimosa board and the SDR to help conclude the feasibility of the SDR design.

Chapter 6 is the final chapter that concludes the research and findings gathered from this project. A section is also provided on the future work that must be completed to see this prototype to a commercial AIS product.

Chapter 2

BACKGROUND

This chapter will discuss the techniques behind SDR receiver architectures, stepping through the signal chain from the antenna all the way to baseband processing. Fundamental principles of SDR receiver systems are covered, addressing digitization of analog signals, important performance measures and down-conversion techniques. In the final section, baseband processing using discrete FM demodulation is derived. This chapter begins by presenting background on the application of AIS.

2.1 MARITIME AUTOMATIC IDENTIFICATION SYSTEM (AIS)

In 2002, the International Maritime Organisation (IMO) brought in a new requirement as a revised version of regulation 19 of Safety of Life at Sea (SOLAS), Chapter V [22]. AIS was created as a collision avoidance tool that would allow commercial vessels to broadcast and receive information for public safety. This navigational equipment was to be carried on-board ships, in accordance to ship type. The regulations required AIS to be mounted aboard all international travelling ships of 300 gross tonnage and upwards, cargo ships of 500 gross tonnage and upwards not engaged in international voyage, and all passenger ships regardless of size. On 31 December 2004, the IMO mandated the use of AIS to improve safety at sea by sanctioning the tracking of vessels using shore base stations.

The principle of AIS is simple. Virtually all commercial ships broadcast and receive a digital message, notifying information on their position, course and speed provided by a built-in GPS receiver. The information can also include identity and its status under the collision regulations [1]. Any vessels within the ships broadcasting vicinity can receive this information and display it either as a text message, or as a graphic, or as an overlay on a chart plotter or radar [23].



Figure 2.1: Illustration of AIS applications [24].

Figure 2.1 shows the use of AIS in heavily congested waters and conditions where line-of sight is not possible, illustrating the motivation behind AIS. Vessel traffic in the North Sea (between England and Belgium) is shown in Figure 2.1a. The need for an organised display of vessel trafficking is obvious. In Figure 2.1b the Auckland Harbour presents topologies where line-of-sight is sometimes not achievable, making RADAR ineffective.

The coverage of an AIS is similar to VHF radios, and can be received over islands, through heavy rain and can deal with most non-line-of-sight situations. This can provide better coverage than RADAR in some condition, or can even enhance a RADAR picture when combined together. One of the major advantages of AIS over radar is the ability to access information on individual vessels, notifying identities and status. AIS gives you a display of targets within your vicinity and warnings of any potential dangers that may approach. There are three different class types of AIS used for collision avoidance, these are listed as follows:

- Class A systems: Targeted for all IMO/SOLAS commercial vessels, these systems use one VHF transmitter capable of 12.5W, providing a range of 20 to 40 nautical miles [25]. The transceiver operates using Self-Organised Time Division Multiple Access (SOTDMA) to continuously update the slot map in memory, organising available slots for transmission [26]. The slot map is used to allocate any AIS signal in the network for transmission. The SOTDMA transceiver effectively reserves a transmission slot by informing other systems before transmitting. Class A also use a VHF Digital Selective Calling (DSC) receiver

to initiate calls to individuals, groups or all stations within range. To provide communications throughout on-board displays and sensor systems, AIS equipment use marine data specifications such as the NMEA 0183 standard.

- Class B systems: Are a smaller, simpler unit than the Class A transceivers, designed for smaller commercial and leisure vessels. Transmission power is restricted to 2W, providing coverage around 5 to 10 nautical miles [25]. Class B units employ either Carrier-Sense TDMA (CSTDMA) or SOTDMA algorithms. CSTDMA transceivers listens to ships transmitting on the slot map to identify unused slots. Information from Class B systems only appear to other ships when there is room on the AIS channel. Class B units on-board small craft are not required to comply with the carriage requirement of SOLAS Chapter V, Regulation 19 [22].
- Receive-only systems: Inexpensive, low power systems that do not have the capability to transmit information to other vessels. These units only receives AIS information from other vessels. Like Class B units, the Receiver-only systems do not comply with the requirements of SOLAS Chapter V, Regulation 19 [22].

2.1.1 AIS Physical Layer

This project focuses on the Class B “CS” systems, particularly the receiver end. AIS transponders communicate autonomously and continuously over two dedicated digital VHF maritime channels, using 161.975MHz and 162.025MHz as the carrier frequencies [26]. However, marine VHF radio range in frequencies from 156.025MHz to 162.025MHz. The International Telecommunications Union (ITU) refer to this as the VHF maritime mobile band. Development of the SDR will target the entire VHF maritime mobile band, opening up opportunities for other maritime applications. Class B “CS” units operate on 25kHz channels with a bit rate of 9.6 kbps [1]. The modulation scheme used over the channel is bandwidth adapted frequency modulated, Gaussian filtered minimum shift keying (FM/GMSK). The data is encoded using non-return-to-zero inverted (NRZI) modulation, which is GMSK coded before it is frequency modulated onto the transmitter [27], Figure 1.6 illustrates this process in the CMX7032. Only one radio channel is necessary for AIS communications, however, each system can use dual channel operations, transmitting and receiving over both TDMA radio channels to avoid interference issues.

Receiver parameters	Required results		
	Result in PER	Wanted signal	Unwanted signal(s)
Sensitivity	20 %	-107 dBm normal ^a -101 dBm extreme -104 dBm normal at ± 500 Hz offset	
Error at high input levels	2 %	-77 dBm	
	10 %	-7 dBm	
Co-channel rejection	20 %	-101 dBm	-111 dBm -111 dBm normal at ± 1 kHz offset
Adjacent channel selectivity	20 %	-101 dBm	-31 dBm normal
Spurious response rejection	20 %	-101 dBm	-31 dBm
Intermodulation response rejection	20 %	-101 dBm	-36 dBm
Blocking and desensitisation	20 %	-101 dBm	-23 dBm (<5 MHz) -15 dBm (>5 MHz)
Spurious emissions	-57 dBm	9 kHz ... 1 GHz	
	-47 dBm	1 GHz ... 4 GHz	

^a Normal and extreme test conditions as defined in 8.2.

Table 2.1: Class B AIS receiver parameters [1].

Design and development of AIS products must comply with the technical standard for AIS, defined by the International Telecommunications Union (ITU). The ITU along with the International Electrotechnical Commission (IEC) have developed rigorous test standards for AIS products to be compared against before commercial release. For Class B “CS” equipment, IEC 62287-1 and ITU-R M.1371-4 specifies the minimum operational and performance requirements, along with methods of testing and required test results [1, 20]. Targeting these performance parameters is essential for AIS product design. Table 2.1 shows the required receiver parameters for Class B. The unit must achieve a specified packet error rate (PER) for each performance parameter under testing conditions [1]. As stated in Section 1.4, this project aims to achieve receiver performance that matches the required AIS specifications, shown in Table 2.1. This performance criteria will help conclude the feasibility of applying SDR technology for AIS applications.

2.1.2 The Existing AIS Design

The existing AIS solution utilizes the CMX7032, which is a AIS Class B “CS” baseband processor with RF synthesisers [9]. The CMX7032 comprises two parallel limiter-discriminator receive paths and one two-point modulation transmit path. The receiver paths are configurable to AIS or DSC operations. The CMX7032 performs signal modulation/demodulation with associated AIS functions, such as training sequence detection, NZRI conversion and high level data link

control (HDLC) processing [6].

In Figure 1.1, the receiver-only structure is shown, demonstrating the typical receiver path for AIS. At the antenna a SAW filter followed by a LNA is used to remove out-of-band noise and amplify the maritime RF signals. The RF signals then split into two channels, where they both get mixed with a LO to down-convert to an intermediate frequency (IF) stage at 45MHz. Here, monolithic filters are used to remove the upper bound frequency components. The second and final down conversion takes place within the FM discriminator stage. The FM IF system incorporates a mixer/oscillator, two limiting IF amplifiers and quadrature detectors [9] to provide the audio signal at the receiver inputs of the CMX.

Using the two receiver paths creates a lot of board complexity and space on the PCB. The process of converting the desired RF signal to an audio baseband signal requires a multitude of analog components. As discussed in Section 1.2, the front end stages to deliver the high sensitivity and selectivity performance can lead to increased costs in the bill of materials (BOM). The motivation of this project is to reduce the BOM and complexity in the front-end by shifting the as much RF processing in the digital domain as possible. Different receiver architectures will be investigated to achieve a software based platform. This will allow more flexibility in the system by utilizing digital signal processing techniques in the software. Hence, different modulation schemes can be programmed to correspond with any RF transmission within the VHF maritime mobile band.

2.2 RF RECEIVER ARCHITECTURE

This section will discuss the receiver's analog front-end, which is a generic term for circuitry from the antenna all the way to, and including, the ADC. There are many different design methods of the front-end, all of which have a common task: To successfully receive an RF signal and condition it for baseband processing. As discussed in Section 1.4, one of the objectives is to minimise the analog processing stages in the analog front-end (AFE) by achieving the signal conversion from RF to baseband without using an IF in the analog domain. It may be possible to avoid the use of an IF stage and directly convert the RF signal to baseband using analog mixers. However, the use of mixers in the analog domain could be avoided all together by directly digitizing the RF signal and implementing the mixer stage digitally. This section will detail and compare, where

possible, different receiver architectures, starting with the superheterodyne receiver currently used in the existing design. The method of direct conversion is then discussed, and finally, the direct digitization receiver used for the SDR platform is described.

2.2.1 Superheterodyne Receiver

The superheterodyne receiver as we know today was first invented by US Army Major Edwin Armstrong in France, during the end of World War 1 [28]. The principle of the superheterodyne receiver revolves around the process of mixing. Mixers are used to multiply the incoming RF signal with a locally generated signal. The instantaneous level of both input signals into the mixer produces a sum and difference product, centring the RF signal at two new frequencies [29]. Figure 2.2 shows the ideal mixing process to convert the RF input to an IF output.

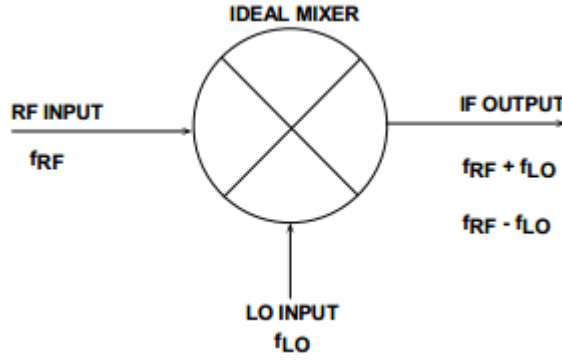


Figure 2.2: An ideal mixing process.

The RF mixer process can be expressed mathematically by expanding the resulting waveform using standard trigonometrical expression. The carrier signal of the RF input and the LO input can be represented by simple sine waves.

$$RF_{input} = A \sin(2\pi f_{RF} t)$$

$$LO_{input} = B \sin(2\pi f_{LO} t)$$

Using a mixer, the two input waveforms are multiplied. This is expressed using the following trigonometric function:

$$\sin(\alpha) \times \sin(\beta) = \frac{1}{2} [\cos(\alpha - \beta) - \cos(\alpha + \beta)] \quad (2.1)$$

Then applying the two input waveforms to the trigonometric expression in Equation (2.1) we get,

$$RF_{input} \times LO_{input} = \frac{AB}{2} [\cos(2\pi(f_{RF} - f_{LO})t) - \cos(2\pi(f_{RF} + f_{LO})t)]$$

From this expression the two terms $(f_{RF} + f_{LO})$ and $(f_{RF} - f_{LO})$ represent the sum and difference frequencies on the output of the mixer. For example, a mixer with two input signals of frequencies $f_{LO}=9\text{MHz}$ and $f_{RF}=10\text{MHz}$ would produce a sum and difference product of 19MHz and 1MHz . By convention, the difference product $(f_{RF} - f_{LO})$ provides the down-conversion, and is applied to fixed frequency IF amplifiers and filters. For this scenario the IF stage is at 1MHz . Therefore, any channel at 1MHz gets passed through the signal chain, and out-of-band signals are rejected [30]. Tuning the superhet receiver is simply done by varying the LO frequency. This process allows the use of fixed frequency filters at a lower frequency rather than variable frequency filters. This enables the use of high performance and low cost filter and gain stages. The ability to convert the incoming RF signal to an IF stage where fixed frequency components are used is the key to the superhet's great selectivity and sensitivity.

Designers must be cautious of unwanted signals that can enter the IF stage. In the previous example the IF stage was located at 1MHz . If an unwanted signal at 8MHz is received at the mixing process with $f_{LO}=9\text{MHz}$ the difference term $(|f_{RF} - f_{LO}| = |8\text{MHz} - 9\text{MHz}| = 1\text{MHz})$ will image the unwanted signal into the IF. Therefore, it is very important to include an image rejection filter before the mixer stage so that both frequencies at $f_{imag} = |f_{LO} \pm f_{IF}|$ do not fall within the IF passband [29]. In practice, RF bandpass filters, typically in the form of SAW filters, are used to perform image rejection preceding the mixer. This is illustrated in Figure 2.3. Using higher IF relaxes the requirement of the image rejection filter, meaning any images created will fall well outside the passband, so lower-order filters can be used. Implementing these receivers requires a good frequency plan so that the IF stage does not become corrupted by the imaged frequencies.

Integrating the superheterodyne receiver for SDR contradicts the characteristics of the ideal SDR design. Because the IF stage uses fixed frequency components the bandwidth limitations of the receiver are restricted to the passband of the channel select filters. This reduces the capability to select different channels simultaneously or the number of channels, that may require different bandwidths. This also takes away the flexibility of processing channels that are broadcast outside

the possible frequency bands of the superheterodyne design, making it very difficult to implement multi-channel, multi-standard operations.

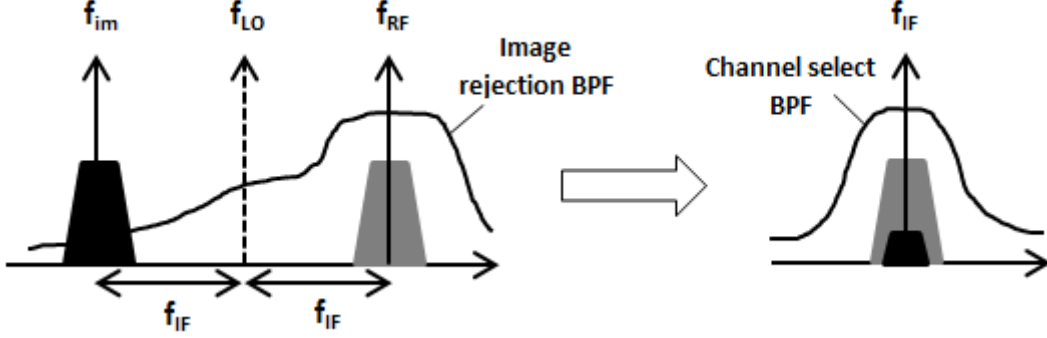


Figure 2.3: Image rejection filter before the mixer, and channel selection filter after the mixer.

2.2.2 Direct Conversion Receiver

The direct conversion receiver, also known as the zero-IF receiver has the capability of converting the RF signal directly to baseband without the need of an IF stage. This method is a more attractive approach, particularly for handset devices where designs are monolithically integrated [30]. The architecture is suitable for systems where power consumption, cost and chip area are the focus of the design. The IF stage is essentially replaced with baseband amplifiers and LPF, reducing the component count. Without the use of an IF stage, image rejection filtering is no longer an issue. As shown in Figure 2.4, the direct conversion receiver makes use of two mixers with their LOs in a quadrature phase relationship, to separate the RF signal into its I and Q components. The two signal paths must be carefully designed to avoid I/Q mismatching, which can lead to corrupted signal constellation [11]. Reliability of these receivers depends heavily on the gain and phase balance between the two signal paths.

The main problem faced when designing a direct conversion architecture is that it suffers from time varying DC offsets. Various phenomena contribute to cause DC offset, such as reflected and refracted signals created from the environment, which inject interfering signals at baseband [29]. A common cause is poorly isolated design of the mixer stage. LO-leakage may be radiated unintentionally through the signal path to a mixer's RF input. Therefore, the mixer creates an unwanted DC offset by mixing its own signal by itself. This effect is heightened when the LO leakage is seen at the input of a LNA, creating an even stronger interferer. Removing DC offset

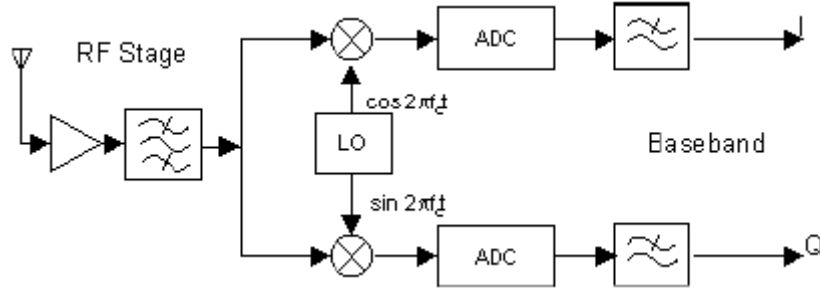


Figure 2.4: [Direct conversion receiver [31].]Direct conversion receiver [31].

is very difficult to implement within the hardware because the LO frequency lies within the receiver bandwidth [31]. Additionally, flicker noise, or $1/f$ noise is also a major baseband noise contributor. Particularly in RF circuits, $1/f$ noise tends to be modulated onto the RF signal, having a spectral response that is proportional to $1/f$ [29].

The direct conversion receiver is an attractive but challenging method to implement. Technologies such as pager, mobile phones and satellite receivers have successfully employed this technique. The integration of this technology is continually developing, and is poised to be used in many more applications.

2.2.3 Direct Digitization Receiver

Directly sampling the RF signal is a step closer to minimizing the analog components in the AFE. The direct digitization architecture consists of band specific gain and passband components. However, the digitization process follows wideband processing. Using superheterodyne or direct conversion receivers, channelization is executed using analog techniques by employing LO(s) to mix the desired channel to an IF or baseband. Direct digitization on the hand, can be used to encapsulate the channelization process within the digital domain by using software to execute functions via a programmable device [32]. This method avoids the use of mixers in the analog domain, eliminating issues that stem from analog RF techniques, such as I/Q mismatching and DC offset etc. Shifting the analog processing into the digital domain fits the design focus for the SDR platform. For this reason, the direct digitization architecture is the chosen receiver method for this project.

Direct digitization heavily relies on the ADC's capability to capture the desired RF signal.

The digitizing process requires a very high sampling rate and a wide bandwidth to successfully sample the incoming signal. Figure 2.5 shows the direct digitization receiver architecture. In the RF stage, the only functional blocks are an antenna followed by the amplifier and BPF. Any interferers that lie within the passband must be handled by the ADC and managed digitally through software.

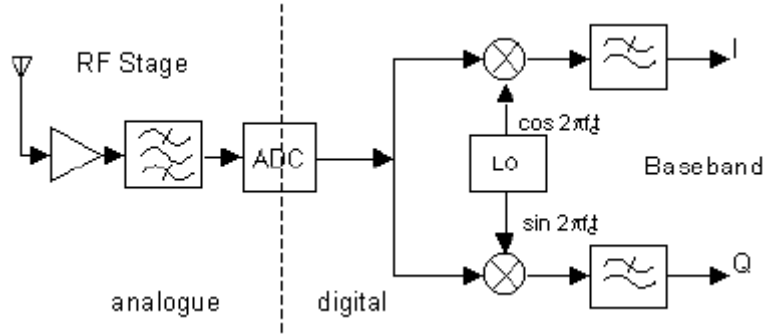


Figure 2.5: Direct digitization receiver [31].

ADC technology has advanced significantly over the past decade. ADC circuitry must be carefully designed to uphold SNR, which is often very challenging to achieve when digitizing RF. The ADC must maintain signal integrity of the desired channel in the presence of interfering signals that may occur in the receiver's pass-band. To condition the incoming signals the AFE must include amplifiers that meet the ADC's input sensitivity. Typically, designers inject enough gain in the front-end so that the signal level at the ADC's input is above the channel noise floor. Applying too much gain such that the levels at the ADC input port exceeds its full scale power specification results in saturating the ADC's output, effectively clipping the digitized waveform. To maintain the signal power for successful analog-to-digital conversion, designers commonly implement automatic gain controllers (AGC) in the front-end. This provides the capability to manage the applied gain.

Applying the direct digitization receiver for maritime applications is a plausible method. Implementing an ADC to capture the maritime signals at VHF is made possible by the present ADC technology. Although, the cost of operating an ADC at these frequencies can be in the range of \$100.00 (USD) [15]. Moreover, capturing the maritime bandwidth of 6MHz will require high resolution to preserve all signals within the digitized bandwidth. As discussed in Section 1.4 This project will investigate digitization techniques such as subsampling that will allow the use of

low cost ADC's for direct digitization receiver's. This research will help identify the performance requirements such as speed and resolution needed by the ADC, and support the designs for the direct digitization receiver used in the SDR prototype.

2.3 DIGITIZATION

One of the fundamental properties of SDR is the expansion of digital signal processing towards the antenna, where traditional analog techniques have been the trend. The design of a software radio that encapsulates all processing digitally is of special interest. Digitization is one of the key methods in attaining a software driven system. Replicating the RF signal digitally is achieved through the concept of discrete time and amplitude sampling of an analog signal. This section will introduce the sampling theorem and also detail methods that can be applied to SDR design to successfully digitize the VHF maritime band.

2.3.1 Sampling Theorem

To capture continuous analog data, samples at discrete intervals must be selected such that an accurate representation of the original signal is obtained. Figure 2.6 displays an analog signal that is sampled at periodic time intervals, t_s . The level of the waveform is represented by amplitude quantization, corresponding to the resolution of the converter. By observation it can be seen that the information between each sample is lost; the more samples captured (ie. higher sample rate) the more accurate the digital waveform is represented. Lowering the sample rate to a point where critical information is lost leads to the statement of Nyquist's Criteria: An analog signal,

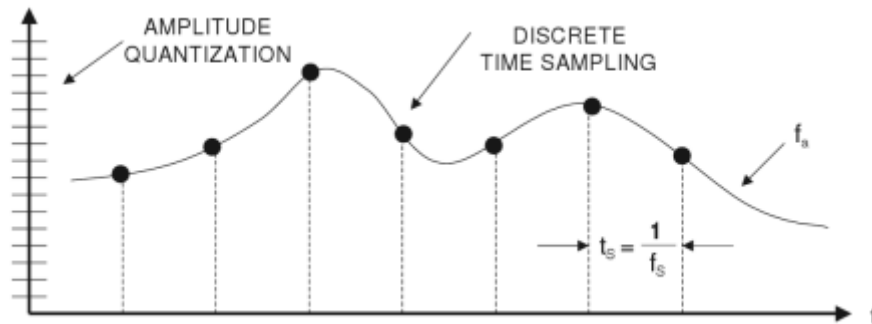


Figure 2.6: Illustration of a sampled waveform [12].

f_a can be reconstructed from a sequence of equally spaced uniform samples if the sampling rate, f_s exceeds twice the highest frequency of the original signal [33]. The Nyquist Criteria therefore requires a sample rate of $f_s \geq 2f_a$ to achieve unambiguous data that avoids overlapping aliased components. This statement presumes a signal with frequency components from DC to some upper bound value, f_a [34].

To get a clear understanding of sample theorem, consider the three time domain figures presented in Figure 2.7. The sine wave represented in the dotted line is the original signal, the periodic dots along the original signal show the samples taken. In Figure 2.7a, where the sample rate is one sample per cycle (ie. $f_s = f_a$) the resultant waveform, shown as the solid line, is a DC signal. Nyquist criteria is violated in this scenario so signal is not preserved. Increasing the sample rate to two samples per cycle or ten samples per cycle as shown in Figure 2.7b and Figure 2.7c respectively meets the Nyquist's Criteria, preserving the structure of the original signal.

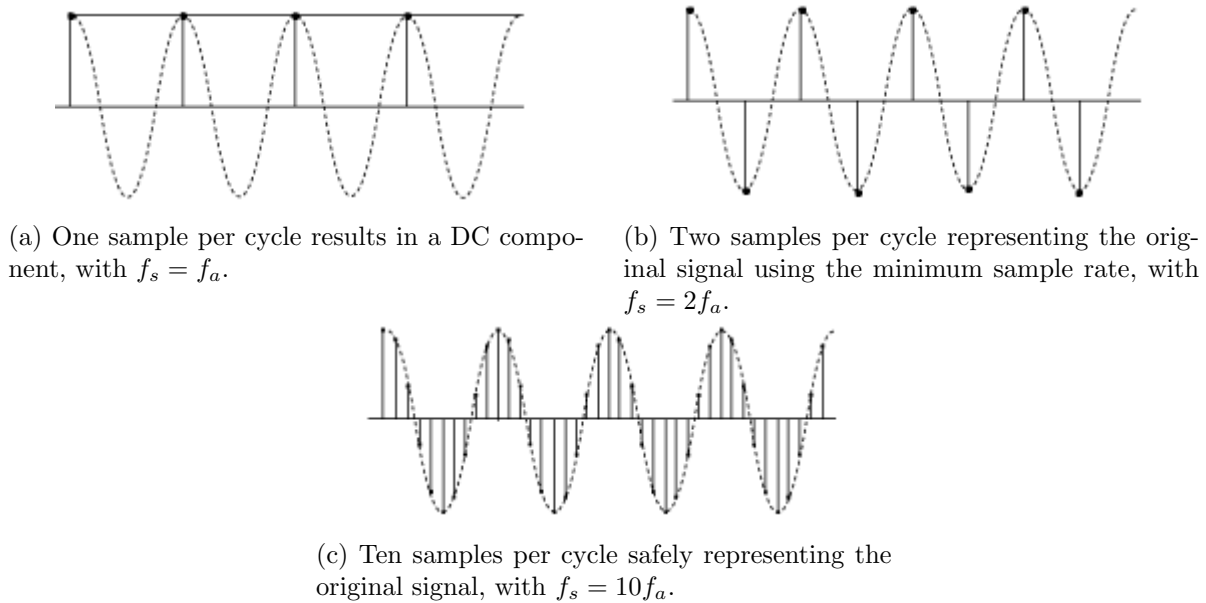


Figure 2.7: Three scenarios of sampling the original signal. Note, the dotted line represents the original signal [35].

The forth scenario displayed in Figure 2.8 shows an interesting phenomena, where the original signal, shown as the blue line, has been reconstructed to form a waveform, shown as the red line, with a lower frequency. This phenomena is known as subsampling, where the original signal has been aliased, presenting a new frequency component. In Figure 2.8 the original signal is sampled

at 1.75 samples per cycle representing a situation where $f_s < 2f_a$, and the information obtained from the samples represents a sinewave having a frequency lower than the original signal. In fact, the reconstructed signal will have a frequency that is lower than $f_s/2$. This is because the original signal's frequency component has been aliased into the Nyquist bandwidth between DC and $f_s/2$, as was shown in Figure 1.4. Observation of the aliased signal into the Nyquist bandwidth can be shown by describing subsampling in the frequency domain.

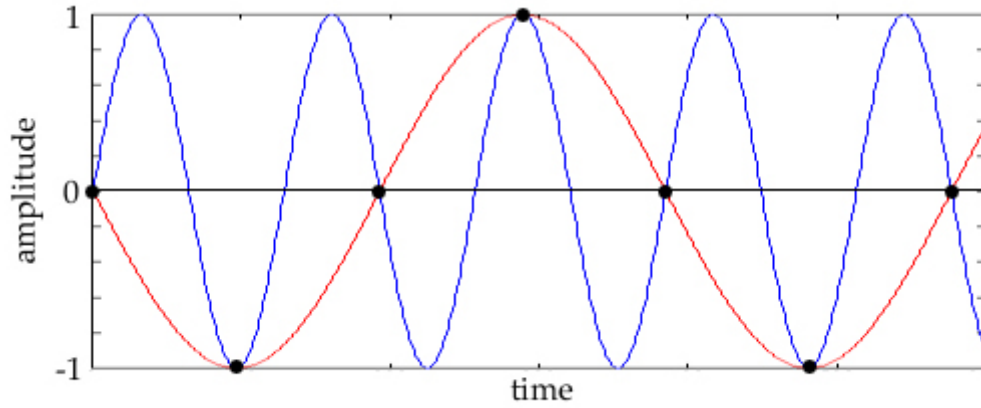
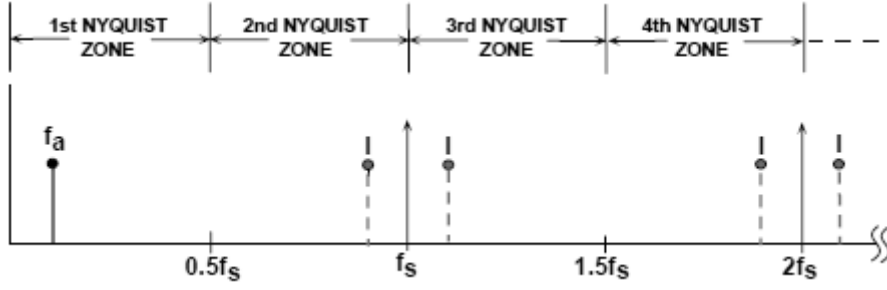
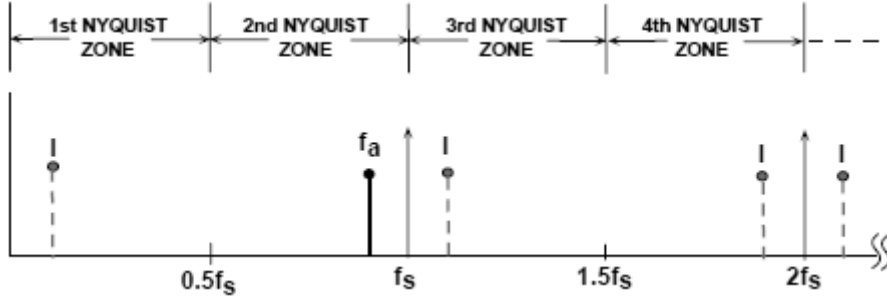


Figure 2.8: An illustration of subsampling. The original signal (shown in blue) is sampled at a rate of 1.75 samples per cycle, the reconstructed waveform presents a lower frequency.

Studying the frequency domain representation of sampling theorem provides a visual of the aliased signals throughout the spectrum. The frequency components displayed in Figure 2.9a shows the spectrum of a system that follows Nyquist's Criteria, where f_a is sampled at a rate greater than $2f_a$. Therefore, the frequency component located at f_a remains in the first Nyquist zone (DC to $f_s/2$). The spectrum shown in Figure 2.9 are divided up into Nyquist's zones, with bandwidths equal to $f_s/2$. Regardless of the incoming signal's frequency, the effect of sampling will capture the original signal and its aliased versions within each of the Nyquist zone's. It is important to note that sampling f_a creates two alias (or image) components of the original signal about each of the sample frequency harmonics (ie. $f_s, 2f_s, 3f_s \dots$). These aliased components are located at $|\pm kf_s \pm f_a|$, where $k = 1, 2, 3, \dots$. In Figure 2.9b the sampling frequency, f_s is only slightly higher than the analog frequency, f_a . The desired signal component at f_a lies outside the first Nyquist zone, however its image component falls inside, at $f_s - f_a$. This effect relates to the time domain illustration shown in Figure 2.8, where the frequency of the reconstructed signal has been reduced, ie. imaged into the first Nyquist zone [34].



(a) The original signal at f_a is sampled at a rate $f_s > 2f_a$. Therefore, the original frequency component is preserved.



(b) The original signal at f_a is sampled at a rate slightly below $2f_a$. Therefore, an alias component is seen in the first Nyquist zone (also referred to as Nyquist bandwidth).

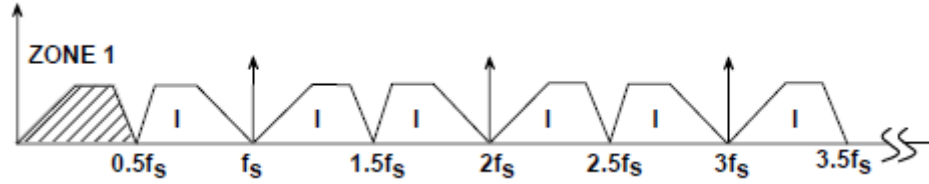
Figure 2.9: Frequency domain representation of sampling theory [34].

Any frequency component, whether it be a spurious tone or random noise, that lie outside the Nyquist bandwidth will be aliased back into the first Nyquist zone. Therefore, anti-alias filtering ahead of the sampler is required in all digitizing applications to remove unwanted aliases that can corrupt the wanted signal [36]. An input signal with a frequency, f_a will require an anti-aliasing filter with a pass band from DC to f_a to remove any signal components above f_a . In band-limited receivers, BPF are typically used so that the bandwidth (or frequencies) of interest are the only signals captured in the Nyquist bandwidth. Digitizing band-limited spectrum leads to the concept of subsampling.

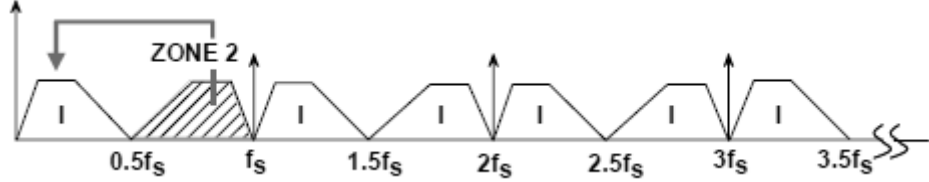
2.3.2 Subsampling

Subsampling, or otherwise known as undersampling or band-pass sampling uses aliasing as an advantage. This method intentionally samples the desired analog signal from outside the Nyquist bandwidth. The image that falls into the first Nyquist zone contains all information of the analog signal, without its original frequency. Figure 2.10 shows three situations where the bandwidth of interest (displayed as a shaded band) is aliased throughout the spectrum. Figure 2.10a shows

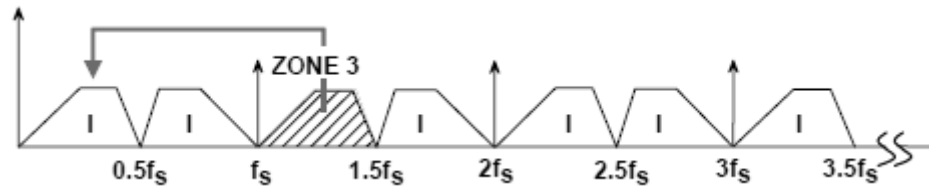
the bandwidth of interest, limited to the first Nyquist zone. After digitization an image appears in each of the other Nyquist zones, all of which are an accurate representation of the original signal. The frequency inversion occurs about each of the sample frequency harmonics. It is possible to recover the frequency components in software to retrieve the original information [33]. Figure 2.10b shows the bandwidth of interest in the second Nyquist zone. This case displays subsampling, intentionally aliasing the signal and inverting the frequency components into the first Nyquist zone. In Figure 2.10c, the location of the wanted bandwidth in relation to the sample frequency aliases an exact replica of the desire band from the third Nyquist zone to the first without any spectral reversal. From this evaluation it can be seen that every odd Nyquist zone represents the original signal without any spectral reversal.



(a) The bandwidth of interest lies in the first Nyquist zone. With $f_s = 2BW$.



(b) The wanted bandwidth now lies in the second Nyquist zone. Therefore, a frequency inverted version aliases into the Nyquist bandwidth (or first Nyquist zone).



(c) Aliasing the wanted bandwidth from the third Nyquist zone aliases an exact replica into the Nyquist bandwidth.

Figure 2.10: Three cases demonstrating the effect of aliasing the bandwidth of interest (the shaded block) within each Nyquist zone [34].

This analysis leads to the re-evaluation of Nyquist's Criteria: The actual minimum sample rate required to obtain unambiguous signal information is a function of the of the signal's bandwidth. To preserve the information of a signal of bandwidth, BW , the sample rate must be greater than or equal to twice the signal bandwidth ($2BW$). This rule is irrespective of the

where the bandwidth may lie within the spectrum, assuming an ideal ADC is being used. The only limiting factor is that the sampled signals are confined to a single Nyquist zone. The aliased components must not overlap each other by entering neighbouring zones [12].

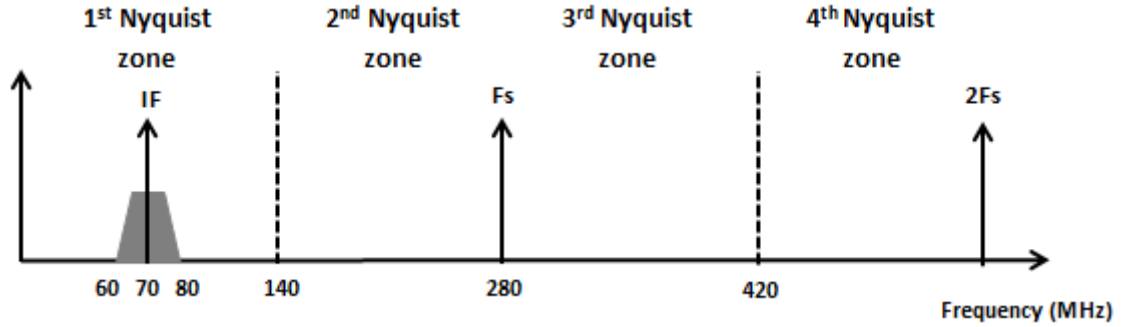
By developing a frequency planning strategy such that the maritime bandwidth lies in a higher Nyquist zone, an image of the maritime bandwidth can be obtained at a lower frequency ie. the first Nyquist zone. Band-limiting the receiver to encompass the maritime bandwidth, and sampling at a rate that positions an odd Nyquist zone ($f_s/2$) over the entire maritime bandwidth, creates an exact aliased replica in the Nyquist bandwidth. For example, if a frequency planning strategy was developed such that the maritime bandwidth lay in the third Nyquist zone, like in Figure 2.10c, an exact representation of the maritime bandwidth will be aliased to the first Nyquist zone. This will allow the hardware platform to perform functions at a more manageable rate.

2.3.3 Oversampling

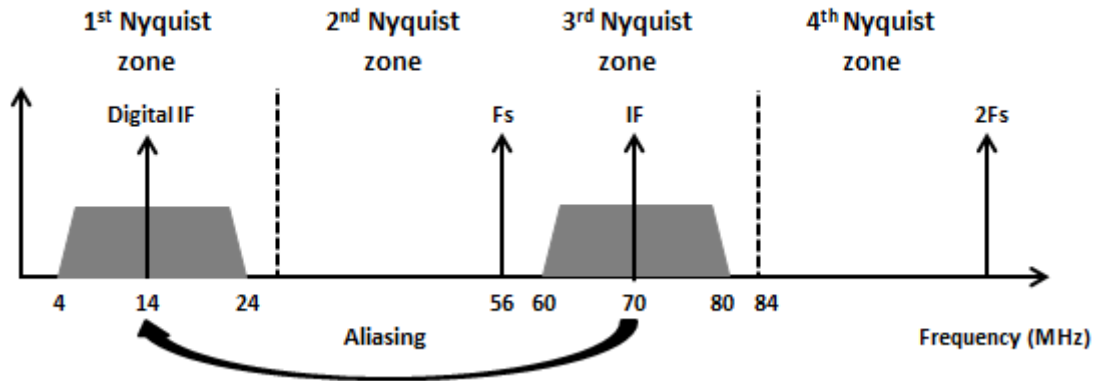
Implementing subsampling allows engineers to reduce the required sample rate so the Nyquist bandwidth ($f_s/2$) is just large enough to contain the signal(s) of interest. Oversampling has the opposite effect, where the Nyquist bandwidth is much larger than the bandwidth of interest. Figure 2.11 compares the sample rates required using oversampling and subsampling for radar applications. The IF generally used in RADAR is 70MHz, with a channel bandwidth of a few kHz to a few MHz [37]. The band of interest is 20MHz centred at 70MHz. By utilizing oversampling, the 20MHz bandwidth can be positioned in the middle of the first Nyquist zone by choosing a sample rate of 280MHz. Figure 2.11a shows the spectrum of the oversampled signal. Comparing Figure 2.11a with a subsampled system as shown in Figure 2.11b, the sample rate can be reduced to 56MHz. Notice the 20MHz bandwidth is now centred at 14MHz within the Nyquist bandwidth (of 28MHz).

Systems that employ oversampling must manage the high sampling rates. Generally, devices such as the a DDC IC chip or an FPGA are used to process the high data output from an ADC [37]. The sample rate used to represent the analog signal dictates the processing speed required. It becomes very difficult to manage power consumption and costs for programmable devices to perform at 280MHz. As the data rates increase, the PCB layout, signal routing and

the placement of high speed devices in the circuit must also be carefully designed [38].



(a) Oversampling the RADAR bandwidth, $BW=20\text{MHz}$ with $f_s=280\text{MHz}$. The digitized bandwidth remains at $IF=70\text{MHz}$.



(b) Subsampling the RADAR bandwidth using $f_s=56\text{MHz}$ aliases the signal components from the third Nyquist zone to the first.

Figure 2.11: Spectral comparison of oversample and subsampling the RADAR bandwidth [39].

However, there are benefits in oversampling. Many applications have resolution requirements relating to the signal's dynamic range, where the slightest variation in the SNR must be measured. The general approach would be to use a higher resolution ADC. However, there are signal processing techniques that can improve the resolution (ie. the effective number of bits (ENOB)) without employing the cost and complexity of expensive ADCs. This can be achieved by oversampling the low resolution ADC, and then post processing the oversampled signal through digital filters and decimators [38]. To understand the significance of oversampling, the relationship between quantization noise and resolution must be discussed.

The resolution of an ADC is the ratio of the full scale voltage range to the number of digital levels (2^N , where N is the number of bits) that reside within the voltage range. This gives a measure of accuracy. The higher the resolution, the more digital levels in the voltage range,

hence, the lower quantization noise [39]. The power spectral density (PSD) of the quantization noise added from an ADC conversion is given by:

$$PSD_{quantnoise} = \frac{(LSB)^2}{12f_s} \left[\frac{W}{Hz} \right] \quad (2.2)$$

The least significant bit (LSB) value is the voltage of the ADC's smallest step size within its voltage range. From Equation (2.2), it can be seen that the quantization noise PSD is reduced by decreasing the LSB value ie. increasing the bit resolution. Alternatively, increasing the denominator by using a higher sample rate can also achieve this. This leads to the notion of oversampling. Observing the PSD in Figure 2.12a we can see that the signal component immersed in quantization noise has a reduced SNR. As shown in Figure 2.12b by increasing the sample frequency the PSD representation of the quantization noise has decreased after oversampling [39]. Increasing the Nyquist bandwidth lowers the aliased quantization noise, and improves SNR. The improvements in SNR is given by:

$$SNR_{oversampling} = 10 \log \left(\frac{f_{OS}/2}{f_{BW}} \right) \quad (2.3)$$

Where, f_{OS} is the oversampling frequency and f_{BW} is the bandwidth of the desired signal. From Equation (2.3) it can be seen that by doubling the oversampling frequency, f_{OS} results in an addition 3dB to the SNR. The theoretical signal-to-quantization noise ratio is based on the quantization error due to the resolution of the ADC [40]. This can be calculated as a function of the ENOB as follows:

$$SNR_Q = (6.02 \cdot ENOB) + 1.77 \quad (2.4)$$

With every additional bit (or ENOB) the SNR_Q is increased by 6.02dB. Furthermore, the additional SNR from oversampling in Equation (2.3) can be added to the signal-to-quantization noise ratio in Equation (2.4) [39].

$$SNR_Q = (6.02 \cdot ENOB) + 1.77 + 10 \log \left(\frac{f_{OS}/2}{f_{BW}} \right) \quad (2.5)$$

Equation (2.5) provides the calculated SNR of the signal component, in the presence of quantization noise within an oversampled Nyquist bandwidth. Figure 2.12b shows the improved noise

floor. Post-processing the digital signal by using a LPF removes the out-of-band quantization noise. Following the LPF with a decimation stage, the signal gets averaged by dividing the sample rate to a lower frequency [38]. The output of the decimator ultimately obtains a higher SNR, improving the accuracy of the low-resolution ADC. The method of digital filtering and decimation is discussed further in Section 2.5.2 and Section 2.5.3.

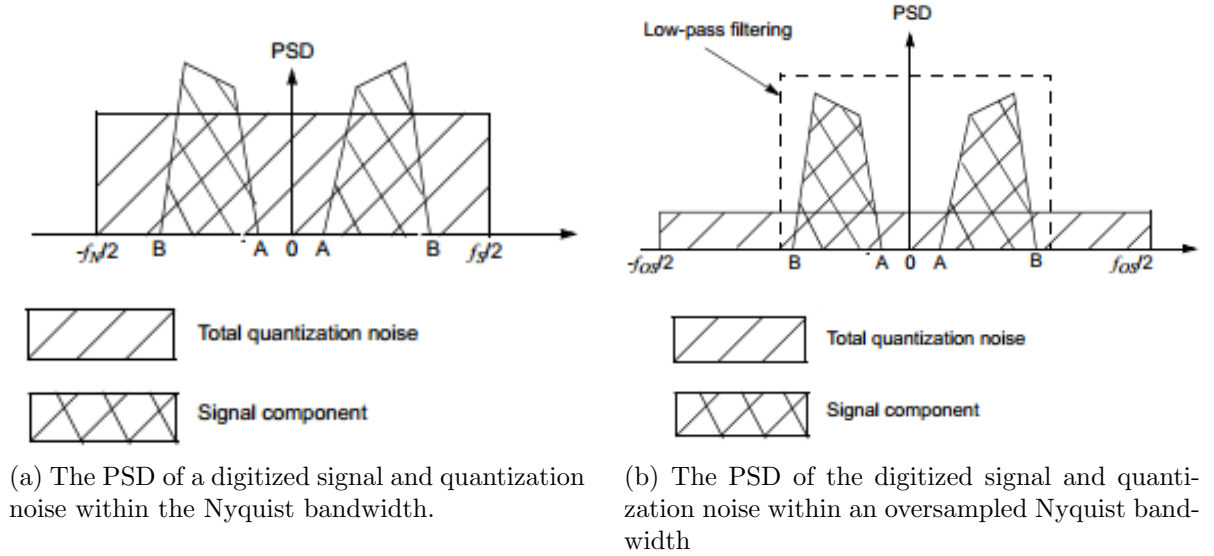


Figure 2.12: Illustration of the reduction of quantization noise using oversampling [39].

2.4 DIGITAL RECEIVER PERFORMANCE PARAMETERS

Since many wideband ADCs are now being implemented in RF applications, performance parameters such as noise figure (NF), SNR, spurious free dynamic range (SFDR), harmonic distortion and jitter have become important design parameters [41]. In general, converter performance is dictated by the processing requirements of the application. Limitations of the ADC occur within two main areas. The first being the on-chip internal circuitry, which can be limited by the slew-rate. As input frequencies increase the stability of the converter decreases [42]. The other limitation is external noise, such as jitter introduced by the clock source used to reference the sample rate. A combination of these factors reduce the ADC's SNR. This section will discuss the performance measures that must be considered when using high speed ADC's.

2.4.1 Sensitivity, Gain and Noise Figure

It is important that receivers have the capability to receive distant signals that have been attenuated millions of times throughout the air interface. The level at which these signals can be received successfully is dictated by the noise levels received at the antenna and those created within the receiver design itself [30]. To improve the signal quality of weak signals, amplification is typically used to provide adequate signal levels for processing. The ratio between the input and output power of an amplifier is known as the gain. The receiver is noise-limited when the gain is sufficiently high enough that the weakest signal level can be processed adequately. This signal level translates to the sensitivity of the receiver. The external noise level at the antenna typically dictates the sensitivity level. However, it is possible for some systems to have external noise fall enough that the sensitivity level corresponds to the internal noise of the receiver [43].

The internal noise of the receiver system is generally measured by noise figure, NF. This provides a measure of the ratio between the total effective input noise power of the ADC and the amount of the noise power caused by the source resistance [43]. Noise figure is often referred to as noise factor, F. Calculating the noise figure of even the best low-noise ADCs, can result in surprisingly high noise figure when compared to typical RF components, such as LNAs and gain blocks, etc. Therefore, designers must be cautious when dealing with ADCs in RF receivers.

To calculate noise figure, the model shown in Figure 2.13 is used. This assumes the ADC input comes from a noise source of resistance, R , which is also band-limited to $f_s/2$. ADC's typically have high input impedances, it is assumed that the input source resistance, R is equal to the input impedance. Figure 2.13 also assumes that the signal input power of a sinewave, $v(t) = V_o \sin(2\pi ft)$, reaching the full scale input range of the ADC with a peak-to-peak amplitude of $2V_o$. The first step in calculating the ADC noise figure, NF_{ADC} is knowing the ADC's full

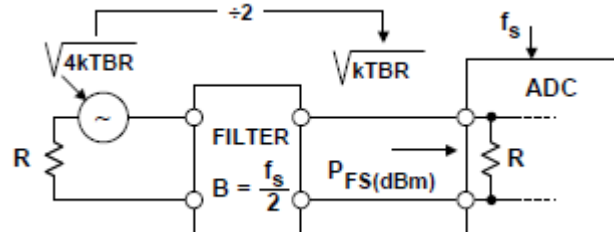


Figure 2.13: Circuit model used to calculate the ADC noise figure [43].

scale power, this can be calculated as:

$$P_{FS} = \frac{(V_o/\sqrt{2})^2}{R} = \frac{V_o^2}{2R} \quad (2.6)$$

An important parameter in the noise figure characteristics is the ADC's rated full scale SNR (or SNRFS), which is typically shown on the ADC data sheet. This provides an indication of the ADC's channel noise floor. The SNR of the ADC can be expressed as follows:

$$SNR = 20\log_{10} \left(\frac{V_{FSrms}}{V_{Noisrms}} \right) \quad (2.7)$$

Where, V_{FSrms} is the ADC's full scale voltage and $V_{Noisrms}$ is the total input rms noise voltage over the Nyquist bandwidth. Rearranging Equation (2.7), an expression for the $V_{Noisrms}$ can be found:

$$V_{Noisrms} = V_{FSrms} \cdot 10^{-SNR/20} \quad (2.8)$$

The next step is to calculate the noise figure. The amount of input voltage noise from the source resistance is $\sqrt{4kTBR}$ divided by two, because of the 2:1 attenuation formed by the ADC input termination resistor [43]. Using Equation (2.8) and dividing by the input voltage noise, an expression for the ADC noise factor, F_{ADC} can be found:

$$F_{ADC} = \frac{V_{Noisrms}^2}{kTRB} = \left[\frac{V_{FSrms}^2}{R} \right] \left[\frac{1}{kT} \right] [10^{-SNR/20}] \left[\frac{1}{B} \right] \quad (2.9)$$

The ADC noise figure, NF_{ADC} , is the ADC noise factor, F_{ADC} expressed in dB. Therefore,

$$NF_{ADC} = 10\log_{10}F = P_{FS(dBm)} + 174dBm - SNR - 10\log_{10}B \quad (2.10)$$

Where the SNR is the rated SNR of the ADC, B is the Nyquist bandwidth ($f_s/2$), k is Boltzmann's constant ($k = 1.38 \times 10^{-23} J/K$), and T is room temperature ($T = 300K$).

System designers must take care when using the noise figure concept in wideband ADCs. Results can be misleading when estimating the total system noise. For instances, Equation (2.9) shows that increasing source resistance, R, can decrease noise factor. However, increased source resistance also increases the circuit noise. A similar effect happens when increasing the

bandwidth, B . This is also contradictory, because increasing the input bandwidth to the ADC increases the input noise [43]. Although, the noise produced by the ADC is much greater than the source noise, so the total system noise stays relatively constant. Therefore, when NF increases the effective circuit noise increases. The overall system noise figure in RF applications affects the sensitivity of the receiver. Use of high noise figure components such as ADC's means the circuitry, particularly in the AFE must be carefully designed with the appropriate low noise, high gain components, so that the rated SNR can be achieved.

2.4.2 Jitter

In the analog-to-digital conversion process of high speed signals, it is necessary to implement a stable clock source as a reference for the sample intervals. The instability in the clock source is known as jitter [44]. Many of the high speed ADCs in today's market employ a sample-and-hold ($S\&H$) circuit that captures samples of the input signal at an instant in time. A sample capacitor is used to record the voltage. Each one half clock cycle, a switch opens or closes to charge or hold the sample capacitor [44]. The variation in the time period the switch opens or closes is known as aperture uncertainty, or jitter. Figure 2.14 shows the slew rate of the ADC is proportional to the clock jitter. The higher the input frequency the more likely the ADC captures inaccurate voltage levels [42]. Mixing the incoming signal with a high jitter clock source results in inaccurate data, compromising the SNR. The effect on the SNR can be observed on the output of the converter.

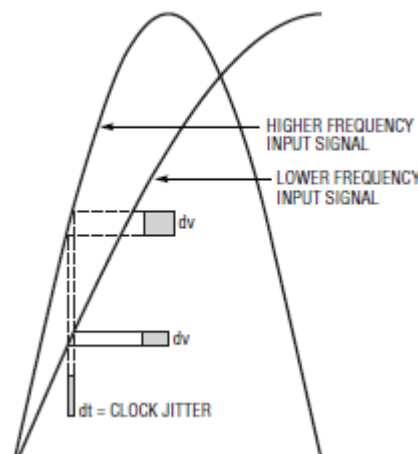


Figure 2.14: The effect of the same jitter on input signals with a higher and a lower frequency. Notice the inaccuracy in voltage level, dv on the higher input frequency when compared to lower input frequency [42].

SNR limitation due to jitter can be calculated as follows [44].

$$SNR = -20\log(2\pi f_a t_j) \quad (2.11)$$

Where f_a is the frequency of the analog input and $t_{j_{rms}}$ is the jitter of the clock in seconds. Given an input frequency and the required SNR, Equation (2.11) can be rearranged to find the clock source performance required to up-hold the SNR of the ADC.

$$t_j = \frac{10^{\frac{-SNR}{20}}}{2\pi f_a} \quad (2.12)$$

2.4.3 Spurious Free Dynamic Range

For wideband converters, one the most important performance parameters is the spurious free dynamic range (SFDR). It defines the ADCs capability to decipher the desired carrier signal from any other noise or spurious frequencies in the digitized spectrum. The measure of SFDR represents the smallest power signal that can be deciphered in the presence of a large interfering signal [45]. SFDR is measured as the range relative to the carrier power and the power of the next significant frequency component, measured in units of dBc. It can also be referenced to the full scale power of the ADC, in units of dBFS [46] as shown in Figure 2.15.

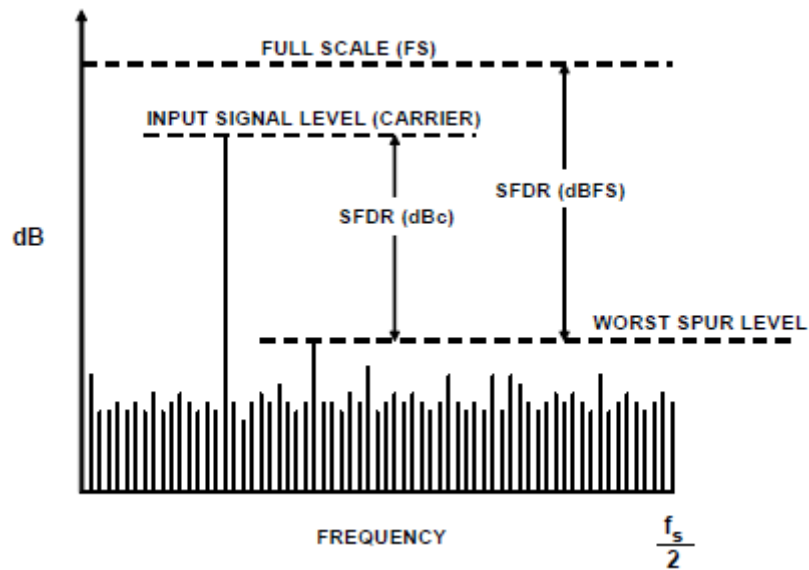


Figure 2.15: Demonstrating SFDR measures in dBc and dBFS [41].

In a well designed ADC, the SFDR is typically dominated by the dynamic range between the carrier and the second or third harmonic. These harmonics are a products of the input signals fundamental frequency, resulting from the clock source and incoming signal. One way to distinguished these harmonic from other interfering spurious by it's location in the spectrum [33]. Figure 2.16 shows the harmonic locations of an input signal with a frequency of 7MHz, sampled at 20MHz. The aliased harmonic components are imaged into the Nyquist bandwidth at frequencies of $|\pm kf_s \pm nf_a|$, where n is the order of the harmonic, and $k = 0, 1, 2, \dots$ Figure 2.16 shows up to the 9th harmonic. By calculating the location of the harmonics designers can determine whether the dynamic range is referenced from a harmonic or some other interfering spurious. The harmonic distortion of the second or third harmonic are typically specified on the data sheet.

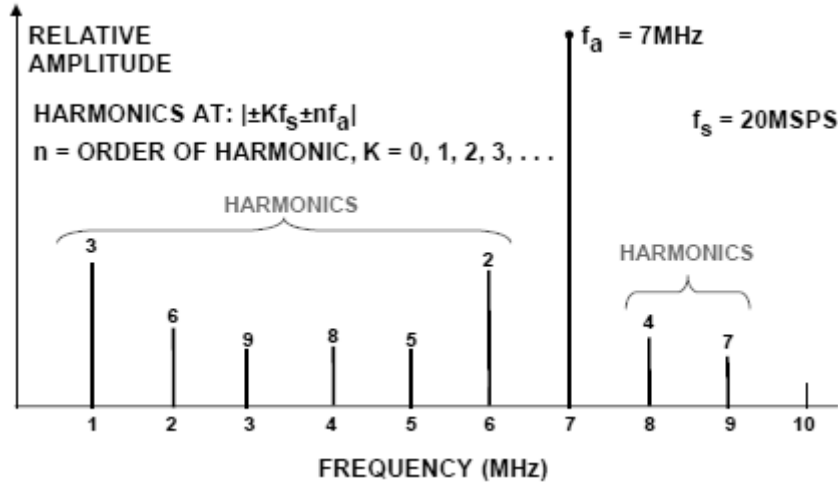


Figure 2.16: Calculating the location of the n th order harmonic [41].

2.5 DIGITAL DOWN CONVERSION

This section continues on from the introduction to the digital front-end (DFE) in Section 1.3.2, detailing the operations behind the algorithms of the DDC. As discussed in Section 1.3.2, the DFE is the stage in the signal chain which processes the real-time data stream digitized by the ADC. The operation of the DFE is to use DDC techniques to down-convert the digitized signal that has been captured within the first Nyquist zone. To get a better understanding of the DDC process, Figure 2.17 provides a model of the signal chain process of a typical communication system. This model includes the baseband signal at the transmitter, $x_{Tx,BB}(t)$, which goes

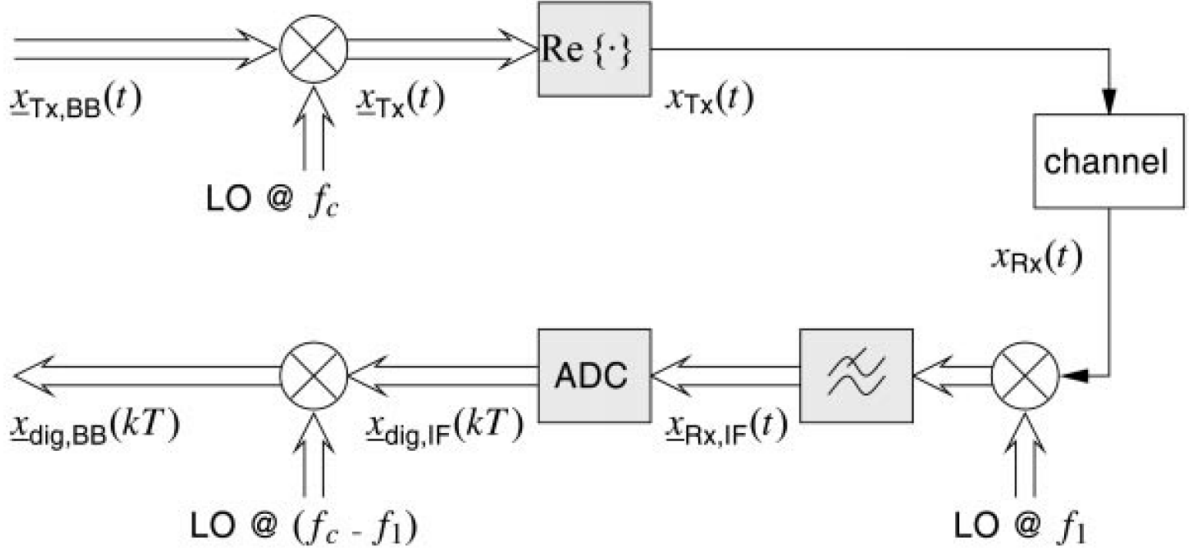


Figure 2.17: Complete signal chain of a communications system [32].

through an up-converter and transmitted as $x_{Tx}(t)$. At the receiver, an IF stage is used in the AFE to down-convert the received signal, $x_{Rx}(t)$, to $x_{Rx,IF}(t)$, which is digitized by the ADC giving, $x_{dig,IF}(kT)$. This model does not account for any distortion, however, it is assumed that the channel introduces adjacent channel interferes over the transmit path [32]. The signal seen at the receiver can be expressed as:

$$x_{Rx}(t) = x_{Tx}(t) + a(t) = \text{Re}[x_{Tx,BB}(t)e^{j2\pi f_c t}] + a(t)$$

$$x_{Rx}(t) = \frac{1}{2}(x_{Tx,BB}(t)e^{j2\pi f_c t} + \hat{x}_{Tx,BB}(t)e^{-j2\pi f_c t}) + a(t) \quad (2.13)$$

Where, f_c is the carrier frequency of the transmitted signal, $a(t)$ is the adjacent channels and \hat{x} is the complex conjugate of x . From Equation (2.13), it can be seen that there are two complex signal components in $x_{Rx}(t)$, located at $-f_c$ and f_c . These signal components (which include $x_{Tx,BB}(t)$) typically lie within the pass-band frequency, B of the receiver's band-pass filter. The LO at the receiver shifts the in-band frequency components to an IF, therefore, the received signal is now expressed as follows [32]:

$$x_{Rx,IF}(t) = x_{Rx}(t)e^{-j2\pi f_1 t}$$

$$x_{Rx,IF}(t) = \frac{1}{2}(x_{Tx,BB}(t)e^{j2\pi(f_c-f_1)t} + \hat{x}_{Tx,BB}(t)e^{-j2\pi(f_c+f_1)t}) + a_{filt}(t)e^{-j2\pi f_1 t} \quad (2.14)$$

Where, $a_{filt}(t)$ represents the adjacent channel in the receiver bandwidth, B and f_1 is the LO frequency. For this example f_1 is treated as $f_1 < f_c$. The frequency components at IF expressed by Equation (2.14) can be observed in Figure 2.18. The channel of interest is centred at IF, which is $f_{IF} = (f_c - f_1)$. It must be noted that the frequency components at $(f_c + f_1)$ are filtered out by the low-pass filter (or band-pass filter) to prevent the ADC from aliasing it into the Nyquist bandwidth. Therefore, the digitized signal is expressed as:

$$x_{dig,IF}(kT) = \frac{1}{2}x_{Tx,BB}(kT)e^{j2\pi f_{IF}kT} + a_{dig}(kT) \quad (2.15)$$

Where, $a_{dig}(kT)$ is the digitized adjacent channels within the receiver bandwidth and T is the sampling period of each sequential (or k th) sample. At the output of the ADC, the DDC does a final down-conversion stage, shifting the channel of interest from digital IF to baseband. The down-conversion is accomplished by multiplying the channel signal with a locally generated digital signal with the respective exponential function:

$$x_{dig,BB}(kT) = x_{dig,IF}(kT)e^{j2\pi f_{IF}kT} \quad (2.16)$$

$$x_{dig,BB}(kT) = \frac{1}{2}x_{Tx,BB}(kT) + a_{dig}(kT)e^{j2\pi f_{IF}kT} \quad (2.17)$$

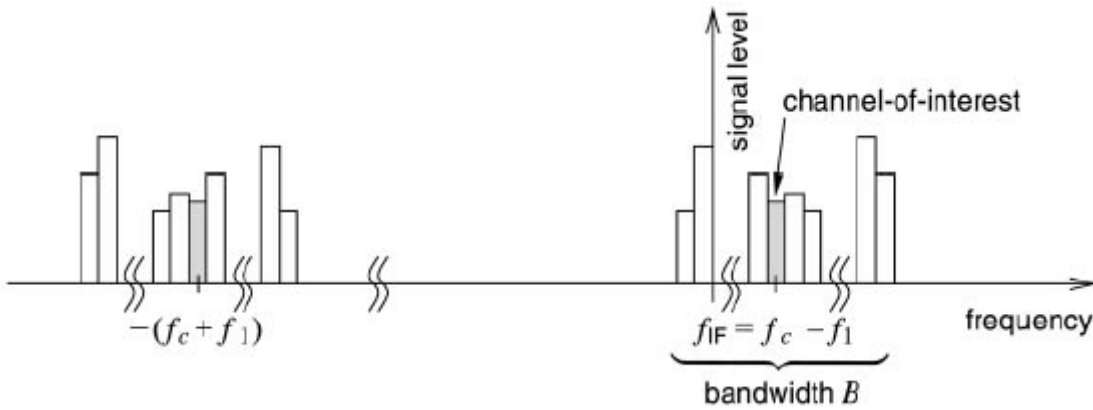


Figure 2.18: The channel of interest at IF in the present of adjacent channels, within the band-pass frequencies of the BPF [2].

Equation (2.17) obtains the digitized version of the transmitted baseband signal, $x_{Tx,BB}(t)$ scaled by $1/2$ [32]. Figure 2.19 shows the channel signal at baseband in the presents of the adjacent channel interferers. Using channelization these interferers can be filtered. This is discussed in Section 2.5.2.

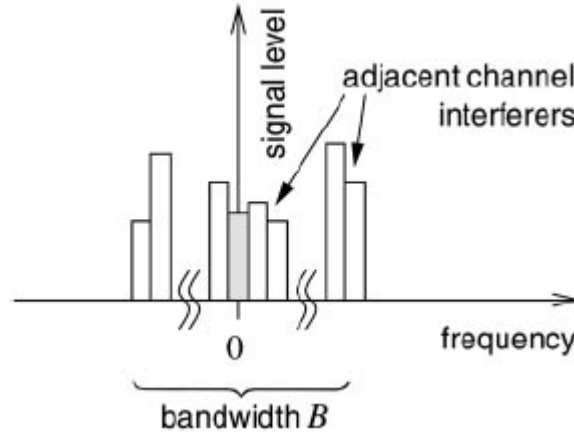


Figure 2.19: The channel of interest at baseband in the presents of adjacent channels [2].

2.5.1 In-Phase and Quadrature Components

The channel component centred at baseband shown in Figure 2.19 must be separated into its real and imaginary component for practical used. The reason I and Q data is so important is that processing a series of sample points of the momentary changes in amplitude in a signal does not always provide enough information about the received signal. Firstly, it is impossible to determine the signal's frequency. It is trivial to calculate the wavelength period, however, this does not provide any indication if it's a positive or negative frequency, i.e. $\cos(x) = \cos(-x)$. This characteristic becomes important when mixing two signals, otherwise the sum and difference products can be misleading if unknown. Secondly, the amplitude of the signal is hard to determine. The peak amplitude of a cosine wave, for example, is located at $0^\circ, 180^\circ, 360^\circ$ etc. However, the amplitude everywhere else is uncertain [47].

The information of a modulated signal can be obtained from the I and Q components, which are observed when looking at a 3D curve of the waveform. Figure 2.20 illustrates a helix of a cosine wave in three dimension. Looking at Figure 2.20 from the side view, the cosine wave is perceived. The 2D projection is shown in Figure 2.21a, which is the “real” signal, corresponding

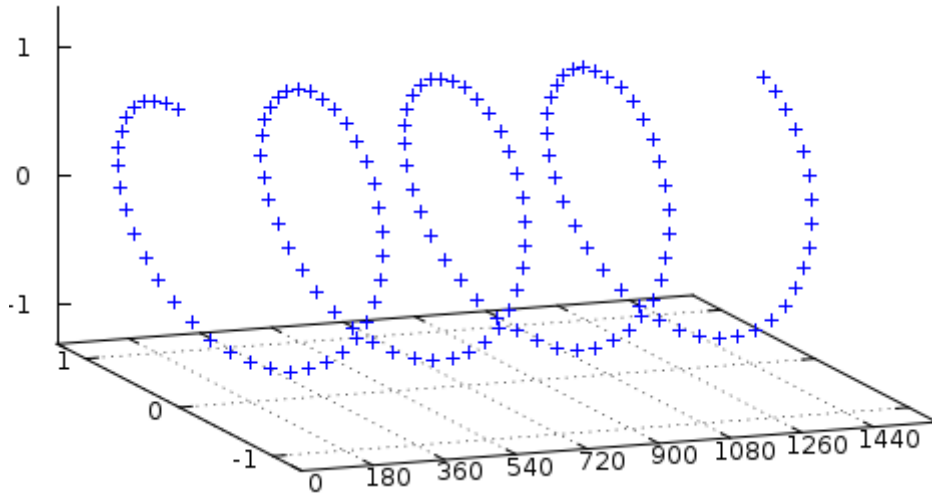
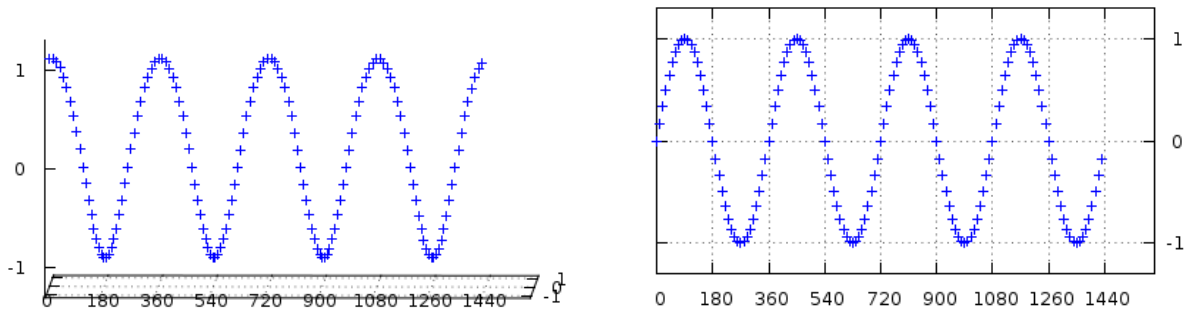


Figure 2.20: Helix representation of a complex signal, demonstrating the I and Q components [47].

to the I component. Viewing the helix from a birds eye view a similar waveform can be seen, as shown in Figure 2.21b. However, it is 90° out of phase. This the “imaginary” signal corresponding to the Q component.

The helix shown in Figure 2.20 shows it winding counter-clockwise, meaning the signal has a positive frequency. If it was wound clockwise the same I data would be represented, but the Q data would show a negative frequency. The peak amplitude of the signal can be determined by the radius of the helix. This can be depicted by looking down the helix waveform from the origin, an illustration is shown in Figure 2.22. The axes are 90° , so the radius (peak amplitude) for every sample can be calculated as $\sqrt{I^2 + Q^2}$. The representation of the I and Q components, as shown in Figure 2.22, display the Cartesian form as two separate variables, a vector of two lengths,



(a) I component of the cosine wave. Looking at the helix from a sideview.

(b) Q component of the cosine wave. Looking at the helix from a birds eye view.

Figure 2.21: Demonstrating the real and imaginary components of a cosine wave [47].

expressed as $I + Qi$. Note that Q is the imaginary part, which has a momentary amplitude of the signal, phase shifted -90° . Every sample of the signal can be described with a peak amplitude, A , times the cosine of some phase angle, ϕ . The value of $A\cos(\phi)$ describes the I component of a single point, and can have any amplitude and/or phase value, provided the signal is continuous. The next sample may have a different amplitude and/or phase corresponding to the modulation of the signal.

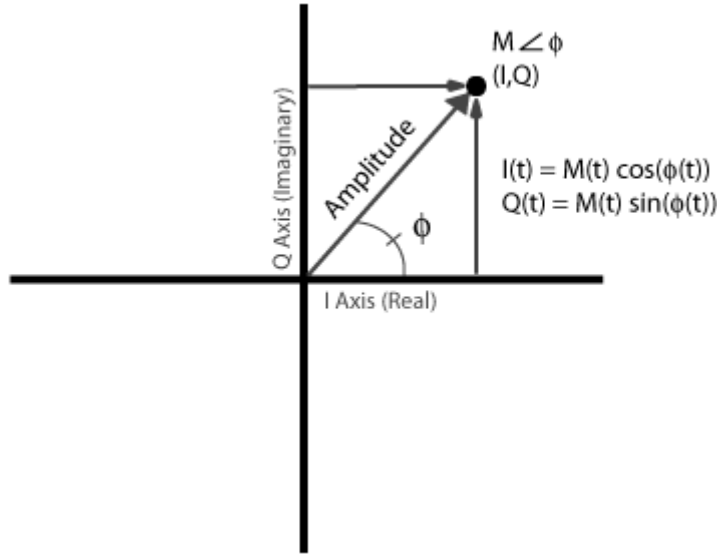


Figure 2.22: Cartesian coordinate system of the I and Q components. View of looking down the helix waveform from the origin [48].

To manipulate the amplitude and phase of a carrier accurately requires expensive modulator hardware. It far more easier to use circuitry for the respective I and Q waveforms. I and Q modulation for RF signals can be described using trigonometric identities. It is known that the carrier is represented by its variables i.e., it's amplitude, A , frequency, f_c and phase, ϕ . The following equation shows the trigonometric identity for a cosine wave with two variables, α and β :

$$\cos(\alpha + \beta) = \cos(\alpha)\cos(\beta) - \sin(\alpha)\sin(\beta) \quad (2.18)$$

Multiplying both sides by amplitude, A and substituting $2\pi f_c$ for α , and ϕ for β , Equation (2.18) is now expressed as:

$$A\cos(2\pi f_c + \phi) = A\cos(2\pi f_c)\cos(\phi) - A\sin(2\pi f_c)\sin(\phi) \quad (2.19)$$

From Figure 2.22 it is shown that the I and Q vectors can be described as:

$$I = A\cos(\phi)$$

$$Q = A\sin(\phi)$$

Where, I is the amplitude of the in-phase carrier and Q is the amplitude of the quadrature-phase carrier. Substituting I and Q into Equation (2.19) yields:

$$A\cos(2\pi f_c + \phi) = I\cos(2\pi f_c) - Q\sin(2\pi f_c) \quad (2.20)$$

This equation describes a modulated RF signal in its I and Q components. Using the I and Q component means that the amplitude, frequency and phase of the carrier signal can be controlled (modulated) by simply adjusting the amplitudes of the I and Q signals (ie. manipulating the magnitude of the I and Q vectors shown in Figure 2.22). Because Equation (2.20) uses a cosine and sine wave, the hardware must employ a 90° phase shift to separate the carrier signal into the I and Q signals. Figure 2.23 shows a diagram used for a typical I and Q modulator. The I and Q data is mixed with a locally generate carrier frequency, where the Q signal is mixed with a 90° phase shifted equivalent and subtracted from the I signal to form Equation (2.20).

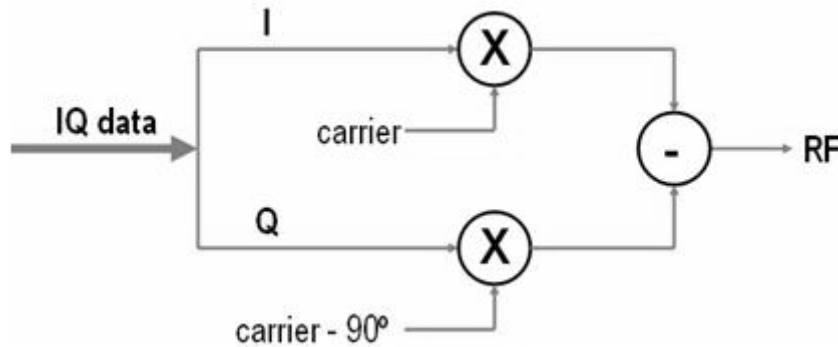


Figure 2.23: I and Q modulator [48].

At the receiver, the I and Q signal can be obtained similarly by mixing the RF or IF signal with the quadrature phase shifted signals. As discussed in Section 1.3.2, the I and Q demodulation process is typically done within the DFE of the SDR. The channel located at the digital IF as shown in Figure 2.18, can be mixed down to baseband in its I and Q components by

implementing a numerical controlled oscillator (NCO). The I and Q data at baseband, as shown in Figure 2.19, can then be filtered and processed to obtain the AIS information.

2.5.2 Digital Filters

The use of digital filtering in SDR design affords better flexibility and performance specifications that would, at best, be very difficult to achieve with an analog approach. The procedure for designing digital filters takes on the same fundamental methods as that for analog filters. Designers must first determine the filter responses to calculate the filter parameters [49]. A digital filter's stopband attenuation, passband ripple and phase response are all characteristics of the order and type of polynomial used to approximate the ideal impulse response [50]. The computation required determines the architecture used to implement the arithmetic. The sample frequency used is a big factor in digital filter implementation, this is because the impulse response is generated as a function of the sample interval, z^{-1} . In order to maintain real-time operations the processor must perform all arithmetic steps within the sample interval so it is ready to process the next sample. The computation time depends on the number of taps in the filter and the speed of the processor, this is the only limitation. Whereas analog filters are component-sensitive, requiring resistors, capacitor, inductors etc. In general as signal frequency increases, the disparity on efficiency increases [50].

There are two fundamental types of digital filters: the finite response filter (FIR) and the infinite response filter (IIR). The difference in the two filters is in the impulse response, as their names suggests. IIR filter utilize feedback ie. use a recursive approach. Therefore, the impulse response extends for an infinite period of time. IIR filters don't match the performance achievable by an FIR filter, and also do not have linear phase. There is no computational advantage achieved on the output of an IIR filter when decimated because the feedback path must be computed every cycle [50]. Therefore, IIR filters are not ideal for SDR operations. The remainder of this section only considers the FIR filters. For a more detailed discussion on IIR filters refer to [49,50].

With FIR filters it is possible to achieve performance levels, such as perfect linear phase response that analog filters can not. Generally, high performance FIR filters require a large number of taps. The addition of more taps to the filter design improves the sharpness of the filter's roll-off. Figure 2.24 shows different roll-off characteristics corresponding to the number of

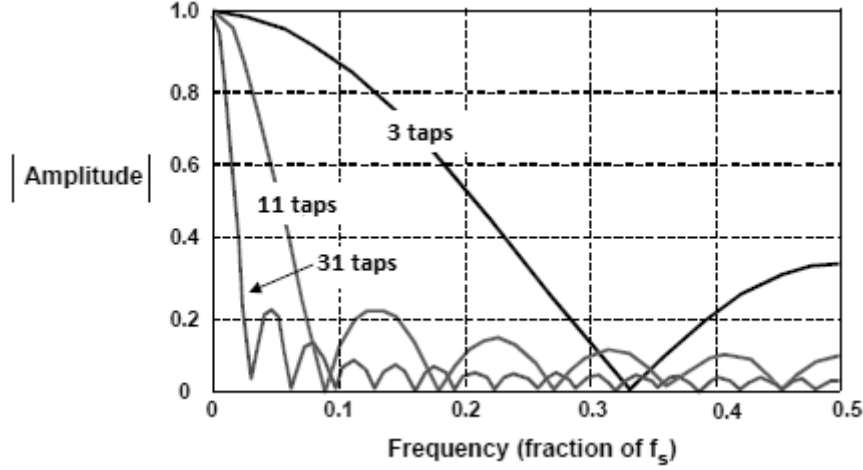


Figure 2.24: Illustration of a filter's roll-off corresponding to the number of taps used [49].

taps (points) used. The essence of designing FIR filters is the appropriate selection of coefficients and the number taps to achieve a transfer function, $H(f)$ for the desired filter response. By calculating the individual coefficients designer can improve not only the sharpness of the roll-off but the attenuation in the stop band as well. The principle of FIR filter design is that the coefficients, $h(n)$ are discrete values that make up the impulse response of the transfer function, $H(f)$. Once the desired filter response is designed the filtered output can be found by convolving the input signal with the transfer function. Figure 2.25 demonstrates this process in both the time and frequency domains.

The general structure of an N -tap FIR filter is illustrated Figure 2.26. Each tap, N in the FIR filter requires a multiply-and-accumulate cycle. The N coefficients are applied sequentially from $h(0)$ to $h(N - 1)$. The associated samples, $x(n)$ pass through the delay line and new samples replacing the oldest each time the summation output is computed [49]. This can be described by convolution shown in the following equation:

$$y(n) = h(n) \otimes x(n) = \sum_{k=0}^{N-1} h(k)x(n - k) \quad (2.21)$$

Where, $h(k)$ is the array of filter coefficients and $x(n - k)$ is the array of input samples to the filter. If the impulse response is designed correctly the FIR filter will attenuate all out-of-band signals so that frequencies in the pass-band are the only signals at the output, as shown in Figure 2.25.

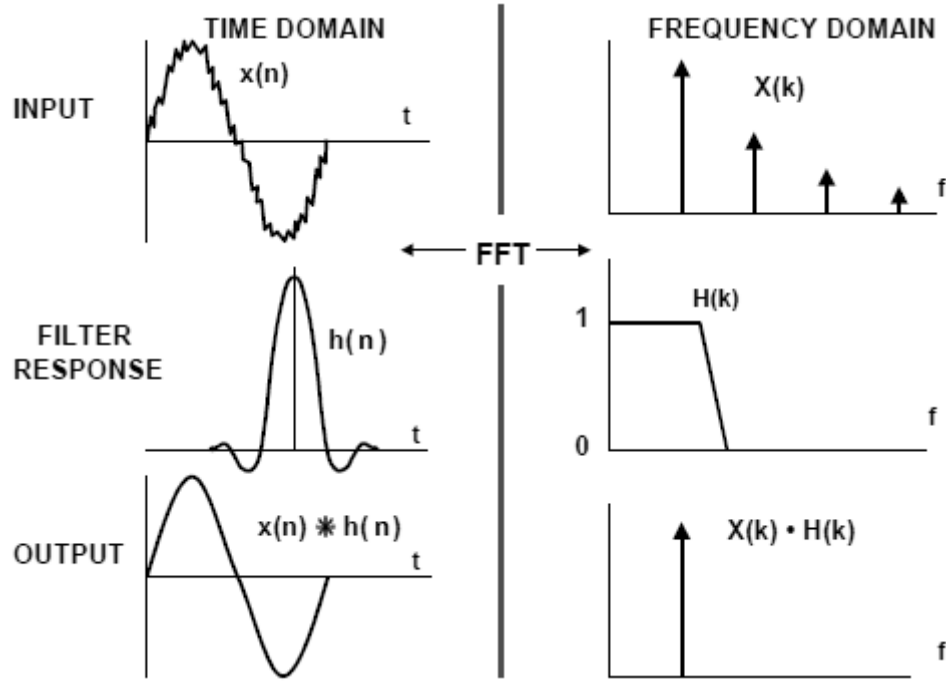


Figure 2.25: The process of an FIR filter in both the time and frequency domain [49].

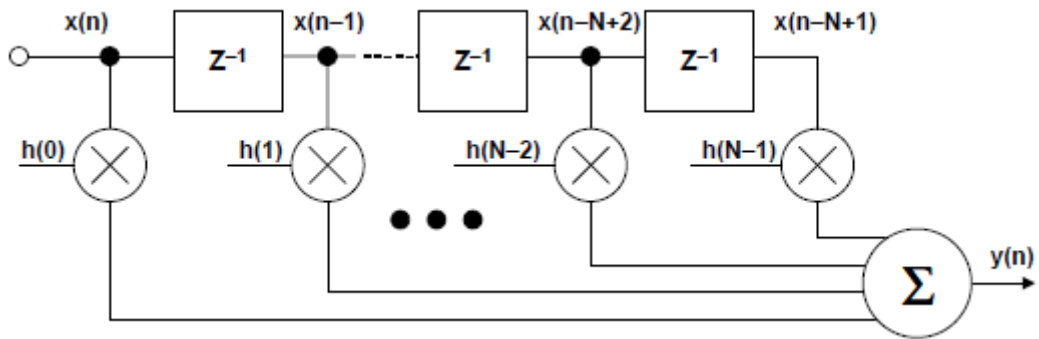
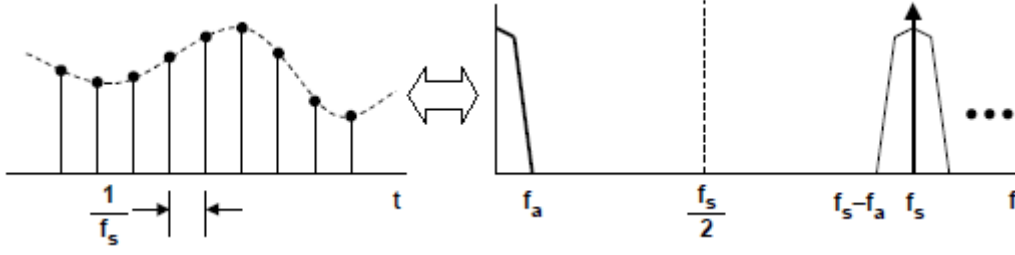


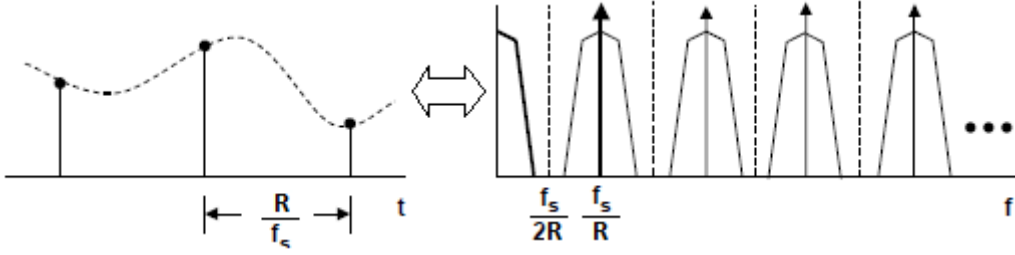
Figure 2.26: A general block diagram of an N-tap FIR filter [49].

2.5.3 Decimation

In digital receivers it is often desirable to reduce the effective sampling rate of the data system. This can simply be achieved by decreasing the sample rates of the ADC. However, in many SDR designs it is desirable to decimate after the input signal has been digitized. The process of decimation, or downsampling a series of sampled values by a factor of R is accomplished by retaining every R th sample and removing the remaining samples [18]. This results in a lower sample rate relative to the original sample rate. In essences, decimation averages the original



(a) Illustrates the time domain (left) and frequency domain (right) representations of the oversampled analog signal, f_a , with a sample rate f_s .



(b) The time domain (left) and frequency domain (right) representation of the decimated signal, with a sample rate f_s/R .

Figure 2.27: Illustration of decimating an oversampled signal by a decimation factor, R [49].

digitizes signal by taking every R th data value. The new sample rate after decimation is:

$$f_{new} = \frac{f_s}{R} \quad (2.22)$$

The expected spectral and discrete time representation of a signal after decimation is shown in Figure 2.27b. The original oversampled signal, f_a is sampled at a rate f_s . The frequency spectrum of this system shows the sample rate is much higher than the minimum requirement of $2f_a$ to preserve the information, as shown in Figure 2.27a. Therefore, it is possible to decimate the digitized signal so that the unused spectrum between f_a and $f_s/2$ can be reduced. The signal decimated shown in Figure 2.27b displays the same signal with a decimated sample rate by a factor R . The signal integrity of the original signal still remains even though the sample rate has been reduced. Designer must insure that the new sample rate f_s/R is slightly greater than $2f_a$, so there is no aliasing components in the Nyquist bandwidth and no information is lost [49].

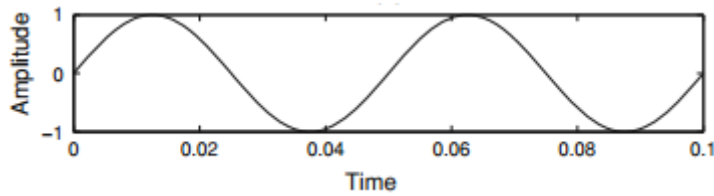
When an application requires the new sample rate, f_{new} to be less than $2f_a$, then a low-pass filter must be employed before decimation so the signal obtains the required bandwidth to avoid unwanted aliasing. Decimation is a very effective approach to improve the SNR by filtering and averaging the digitized signal. As discussed earlier in Section 2.3.3, reducing the

digitized bandwidth through decimation reduces the quantization noise, providing process gain. Other benefits include the reduction in process speed. This designs for the SDR will seek to take advantage of these characteristics in the development of the prototype.

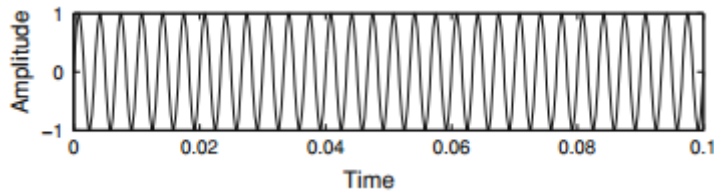
2.6 FREQUENCY MODULATED SIGNALS

Frequency modulation (FM) is commonly used to broadcast over VHF channels. It is used to encode information onto a carrier signal by varying the instantaneous frequency. Figure 2.28 illustrates the relationship between the message signal (shown in Figure 2.28a) and the carrier signal (shown in Figure 2.28b) to form the FM signal (shown in Figure 2.28c). Modulating the carrier with the message signal involves deviating the carrier frequency. If a sine wave is used as the message that deviates the carrier, the expression for the instantaneous frequency is:

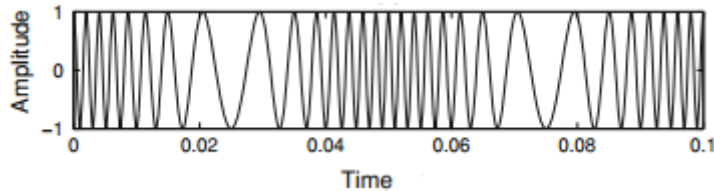
$$\omega_i = \omega_c + \Delta\omega \sin(\omega_m t) \quad (2.23)$$



(a) The message signal, represented as a 20Hz sine wave. This signal is to be modulated into the carrier wave



(b) The carrier signal, represented as a 300Hz sinewave. This signal is used to carry the message signal through the airwaves.



(c) The FM modulated signal. Illustrating the deviation in the carrier frequency that represents the message signal.

Figure 2.28: An illustration of a message signal frequency modulated onto a carrier wave.

Where, ω_i is the instantaneous frequency, ω_c is the carrier frequency, $\Delta\omega$ is the carrier deviation and ω_m is the modulating frequency. Equation (2.23) describes a signal changing sinusoidally about some average frequency. The amplitude of the modulating signal is defined by the deviation of the carrier, and the rate of the carrier deviation is governed by the message frequency. The sine operator in Equation (2.23) is expressed with phase, ϕ not frequency. Thus, the instantaneous frequency must be expressed in terms of instantaneous phase. Measuring the instantaneous frequency of a sinusoidal signal is computed by taking the derivative of the signal's instantaneous phase [18]. This shown in the following expression:

$$\omega = 2\pi f = \frac{d\phi}{dt} \quad (2.24)$$

An expression can be formed to find the instantaneous phase by integrating the instantaneous frequency.

$$\phi = \int \omega_i dt = \int (\omega_c + \Delta\omega \sin(\omega_m t)) dt = \omega_c t - \frac{\Delta\omega}{\omega_m} \cos(\omega_m t) = \omega_c t - \frac{\Delta f}{f_m} \cos(\omega_m t) \quad (2.25)$$

As described in Equation (2.20), a modulated signal is expressed by amplitude, frequency and phase. Therefore, Equation (2.25) can be substituted into Equation (2.20) to form an FM signal.

$$y_{fm}(t) = A \cos(\omega_c t - \frac{\Delta f}{f_m} \cos(\omega_m t)) \quad (2.26)$$

The FM modulation index, β is defined as the ratio of the carrier deviation, Δf to the modulation frequency, f_m .

$$\beta = \frac{\Delta f}{f_m} \quad (2.27)$$

Therefore, an expression for the FM signal can be expressed as:

$$y_{fm}(t) = A \cos(\omega_c t - \beta \cos(\omega_m t)) \quad (2.28)$$

The level of carrier deviation is important in many aspects. The bandwidth of the overall signal is regulated by the deviation. Wideband applications such radio broadcast stations over the 88.5 to 108MHz spectrum typically use a carrier deviation of $\pm 75kHz$. This supports a high

quality message transmission, which occupy a bandwidths of around 200kHz [51]. Narrowband FM applications, such as AIS, generally deviate the carrier around $\pm 3kHz$ or slightly more. The quality of information is not as important for these applications so less spectrum is used.

2.6.1 Discrete FM Demodulation

In DSP based communication systems, complex-signal (quadrature) processing is very useful. As discussed in Section 2.5.1, the I and Q components provide a measure of the magnitude, phase and frequency of a signal at a given instance in time. The purpose of instantaneous measurements in discrete value systems can be very meaningful, particularly when characterising a complicated signal, like a modulated sine wave. For discrete FM demodulation, instantaneous measurements begins by detecting not frequency, but the phase of the incoming signal. Because I and Q components represent the incoming signal as a vector, the phase of the incoming signal can be found by computing the angle of the vector. This was illustrated in Figure 2.22. By using trigonometry, the angle can be calculated as follows:

$$\phi(n) = \tan^{-1} \left(\frac{Q(n)}{I(n)} \right) \quad (2.29)$$

Computing the instantaneous phase requires the arctangent operation, which is difficult to implement without considerable computation resources [18]. Typically, look-up table will be used to find the arctangent. As shown in Equation (2.24), the instantaneous frequency can be expressed as the derivative of the instantaneous phase. The output of the arctangent operator can be converted to a FM demodulated signal by feeding it through a differentiator filter, as shown in Figure 2.29.

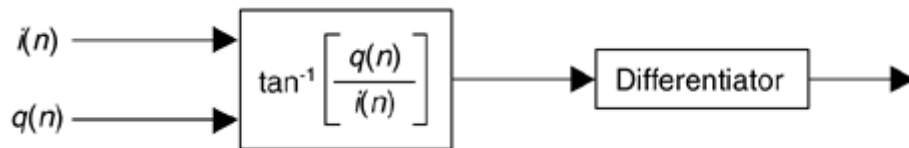


Figure 2.29: Discrete FM demodulation using the arctangent operator and differential filter [18].

This is the traditional approach for discrete signal FM demodulation. However, it is also possible to compute the instantaneous frequency without the use of the arctangent operator, thereby

minimizing the computational resources needed to execute FM demodulation. The algorithm used is based on the following continuous-time variables.

$i(t)$ = in-phase component.

$q(t)$ = quadrature component.

$\phi(t)$ = instantaneous phase = $\tan^{-1}[q(t)/i(t)]$.

$\Delta\phi(t)$ = time derivative of $\phi(t)$ (the instantaneous frequency).

For this expression the assumption is that the $i(t) + jq(t)$ signal is centred at baseband. Initially, the derivative of the arctangent is calculated by using the calculus identity of the time derivative for $\tan^{-1}[q(t)/i(t)]$. Firstly, let $r(t) = q(t)/i(t)$.

$$\Delta\phi(n) = \frac{d\tan^{-1}[r(t)]}{dt} = \frac{1}{1 + r^2(t)} \frac{d[r(t)]}{dt} \quad (2.30)$$

This is essentially the output of the differentiator in Figure 2.29. Substituting $r(t) = q(t)/i(t)$ into $d[r(t)]/dt$ in Equation (2.30) the calculus identity for the derivative of a ratio can be found,

$$\frac{d[r(t)]}{dt} = \frac{d[q(t)/i(t)]}{dt} = \frac{i(t) \frac{d[q(t)]}{dt} - q(t) \frac{d[i(t)]}{dt}}{i^2(t)} \quad (2.31)$$

And so, Equation (2.31) can be substituted into Equation (2.30) to give,

$$\Delta\phi(n) = \frac{1}{1 + r^2(t)} \frac{i(t) \frac{d[q(t)]}{dt} - q(t) \frac{d[i(t)]}{dt}}{i^2(t)} \quad (2.32)$$

Replacing $r^2(t)$ in for $[q(t)/i(t)]^2$ in Equation (2.32) we now have,

$$\Delta\phi(n) = \frac{1}{1 + [q(t)/i(t)]^2} \frac{i(t) \frac{d[q(t)]}{dt} - q(t) \frac{d[i(t)]}{dt}}{i^2(t)} \quad (2.33)$$

Finally, the numerator and the denominator are multiplied by $i^2(t)$ and t is replaced with the time variable index n , resulting in the expression,

$$\Delta\phi(n) = \frac{i(n) \frac{d[q(n)]}{dn} - q(n) \frac{d[i(n)]}{dn}}{i^2(n) + q^2(n)} \quad (2.34)$$

From Equation (2.33) it is noted that the sum of squared in the denominator represents the magnitude of the of the complex signal. If the $i(n) + jq(n)$ is purely FM and hard limited such that $i^2(n) + q^2(n) = \text{Constant}$, then the denominator in Equation (2.33) does not need to be expressed [18]. This expression is more computationally efficient than the use of the traditional method of using the arctangent operator. Therefore, the development of baseband processing will investigate this approach to recover the AIS audio signal.

Chapter 3

DEVELOPMENT OF THE ANALOG FRONT-END PROTOTYPE

The primary goal for the analog front-end (AFE) prototype is to develop a direct digitization receiver, that implements subsampling on the maritime band of signals. The designs will be influenced by the IEC 62287-1 AIS receiver standards [1] to determine if the SDR is a feasible system for collision avoidance applications. With the growth of high speed ADC devices, the capability to capture and process high data rates has been recognized. Thus, an investigation into ADC's is presented in this chapter to identify a suitable device for the AIS receiver. As discussed in Section 2.2.3, the method of directly sampling the RF signal is not commonly employed without an intermediate frequency (IF) stage [52]. Therefore, innovative methods must be designed to meet the required receiver performance. Continuing from the discussion in Section 1.3.1, this chapter will describe the developments of a direct digitization receiver architecture. Discussion on frequency planning strategies to successfully subsample the maritime bandwidth will provide reasoning on why the direct digitization receiver is a practicable approach for AIS applications.

This chapters aims to present a proof of concept for the direct digitization receiver, to provide support in the development and construction of an AFE prototype. Where possible, performance parameters measured from evaluation boards and the prototype will be compared to datasheet specifications and calculated values. Implementation of an AFE will provide the first step in evaluating and developing the SDR platform.

3.1 UTILIZING SUBSAMPLING FOR AIS

In order to apply subsampling successfully, a frequency planning strategy must be developed [53]. Because AIS is only interested in the spectrum for maritime applications, the SDR designs can

be constrained by band-limiting the system to these frequencies only. The maritime bandwidth covers 6MHz and is centred at 159.025MHz. There are a multitude of channels that lie within this bandwidth, specific to maritime applications. These are narrowband channels spaced 50kHz apart from each other to avoid interference, each channel has a bandwidth of up to 25kHz ($\pm 12.5\text{kHz}$ about the carrier) [54]. Therefore, the SDR must have the capability to process multiple narrowband channels that lie at arbitrary frequencies within the bandwidth. The band-limited characteristics allows anti-aliasing filters to be used so that the maritime bandwidth can be safely aliased throughout the spectrum.

The key to subsampling is to create images of the maritime bandwidth within in each Nyquist zone without aliasing over neighbouring frequency components [34]. This is very important to consider when developing a frequency planning strategy. As discussed in Section 1.3.1, the minimum sample rate to preserve the maritime bandwidth, according to Nyquist Theorem, is 12MHz. Therefore, each Nyquist zone ($f_s/2$) will occupy 6MHz. To identify if the aliased components are overlapping it is important to identify the location of the original signal in relation to the sample frequency harmonics. The illustration shown in Figure 3.1 shows that the minimum sample rate of $f_s=12\text{MHz}$ does not encompass the maritime bandwidth within the Nyquist bandwidth.

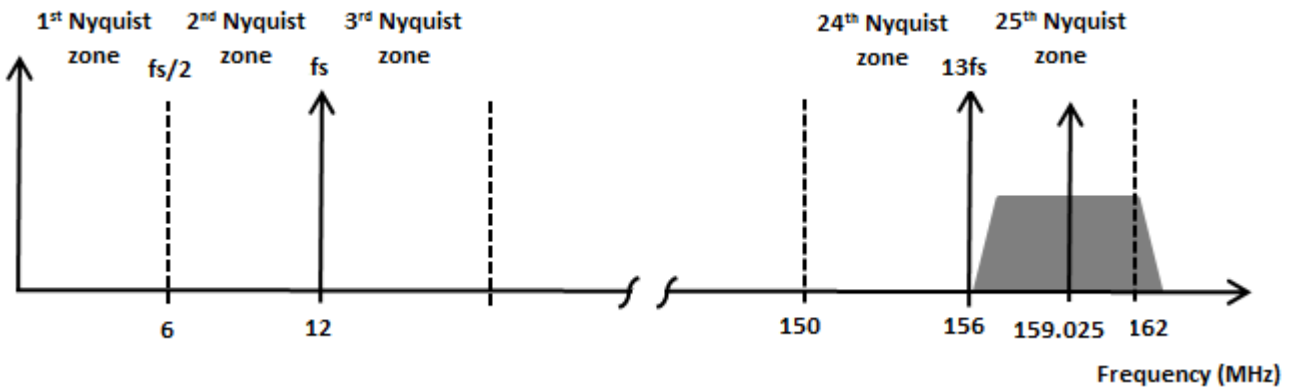


Figure 3.1: Nyquist zones corresponding to a sample rate of $f_s=12\text{MHz}$.

Taking a closer look at the spectrum shown in Figure 3.1 we can see that the position of the maritime bandwidth does not lie completely within the 25th Nyquist zone. The highest frequency in the maritime bandwidth is 162.025MHz, which exceeds the 25th Nyquist zone. The 162.025MHz channel will alias (or “fold”) back into the Nyquist bandwidth once it is sampled.

To illustrate the importance of maintaining all desired signals within the Nyquist zone let's take a look at the spectrum shown in Figure 3.1 after it has been sampled by $f_s=12\text{MHz}$. Figure 3.2 shows the alias components overlapping in the black areas. The 162.025MHz channel get spectrally inverted (or “folded”) into the Nyquist bandwidth, and will alias onto the 161.975MHz channel, interfering with the signal. Any signal at 156.025MHz are clearly within the Nyquist zone so the aliased component has preserved the original signal.

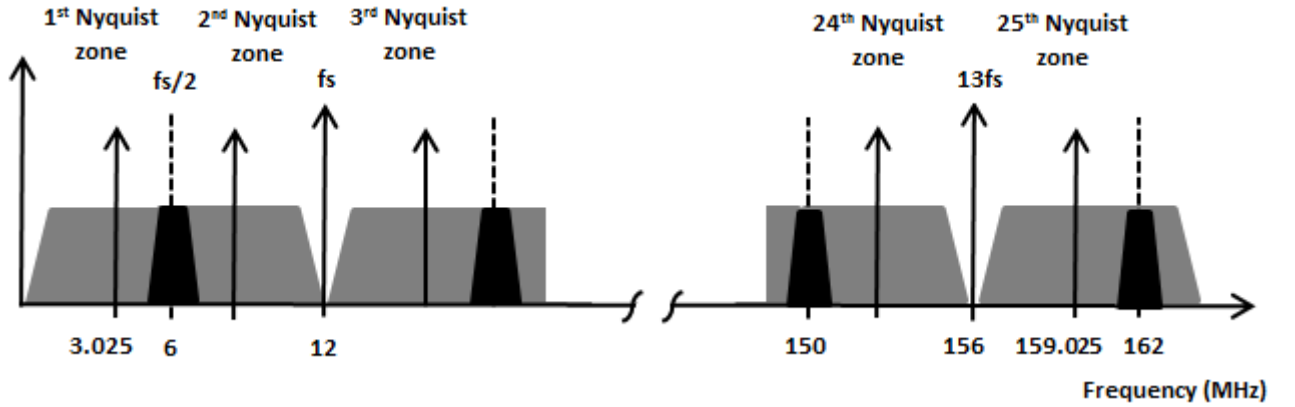


Figure 3.2: Overlapping alias components throughout the Nyquist zones with $f_s=12\text{MHz}$.

From Figure 3.2 we can also get a good understanding on how important an anti-aliasing filter is for subsampling systems. Use of a sample rate that captures the maritime band only means the neighbouring aliased components will be very close together. This relies heavily on the performance of the anti-aliasing filter to attenuate any out-of-band signals at the cut-off frequencies. If the anti-aliasing filter has a large roll-off in its response, noise and interfering signals can potentially alias (or overlap) onto the desired bandwidth, resulting in a similar effect shown in Figure 3.2.

Developing a good frequency planning strategy revolves around the positioning of the Nyquist bandwidth in relation to the desired signal [55]. It is important to obtain a large enough Nyquist bandwidth such that all desired signals are captured. Good design of frequency planning starts with the filter response of the anti-alias filter, rather than the desired bandwidth. The frequencies presented to the ADC input by an anti-aliasing filter (BPF) will ultimately determine the minimum sample rate to avoid noise or neighbouring signals to alias onto the wanted signal. High performance analog filters are difficult to implement at RF, so any large roll-offs in the filters transition band must be accounted for. Frequency planning does not only involves the

preservation of the original signal in the Nyquist bandwidth, but also considers improvements to the quantized signal via post-processing. In Section 2.3.3, the addition of process gain to the receivers SNR can be accomplished by using a higher sample rate to reduce quantization noise in the digitized bandwidth, this leads to the concept of oversampling.

3.1.1 Benefits of Oversampling the Bandpass Signal

Increasing the sample rate results in a larger Nyquist bandwidth. As discussed in Section 2.3.3, this reduces the quantization noise that gets aliased, lowering the ADC noise floor. The effect of increasing the Nyquist bandwidth is advantageous in frequency planning, because it means that a lower n^{th} Nyquist zone can be used to capture the the desired bandwidth. In Figure 3.2, the 13th sample frequency harmonic was used, which represented the 25th Nyquist zone. In subsampling systems it is good practice to reduce the number of Nyquist zones needed to represent the signal. The higher the n^{th} Nyquist zone used, the more quantization noise throughout the spectrum that gets aliased into the Nyquist bandwidth ($f_s/2$) [37,56].

Introducing oversampling to the subsampling frequency plan shown in Figure 3.2 the maritime bandwidth can be aliased safely without overlapping. When applying oversampling there is a trade-off between improving the SNR by increasing the Nyquist bandwidth and the cost of using a high speed ADC. It must be noted that one of the primary goals is to lower the cost of the existing receiver front-end. Therefore, the cost per ADC must be considered. With this in mind, investigation of the ninth Nyquist zone to alias the maritime bandwidth is conducted. To alias the ninth Nyquist zone, four sample frequency harmonics will have to be used. To create the fourth harmonic at 156MHz a sample rate of 39MHz is chosen. The resulting spectrum is shown in Figure 3.3. The maritime bandwidth centred at 159.025MHz gets aliased without any overlapping components.

Oversampling not only helps avoid overlapping aliased components, the increased bandwidth allows the removal of out-of-band quantization noise, accomplished through post-processing [57]. As discussed in Section 2.3.3, post-processing in the digital domain through the use of digital filters and decimation can add processing gain, improving the SNR. From Equation (2.3), the process gain obtained through oversampling can be calculated. Implementing oversampling with a sample rate 39MHz, the SDR digitizes a bandwidth of 19.5MHz, however, the AIS channels of

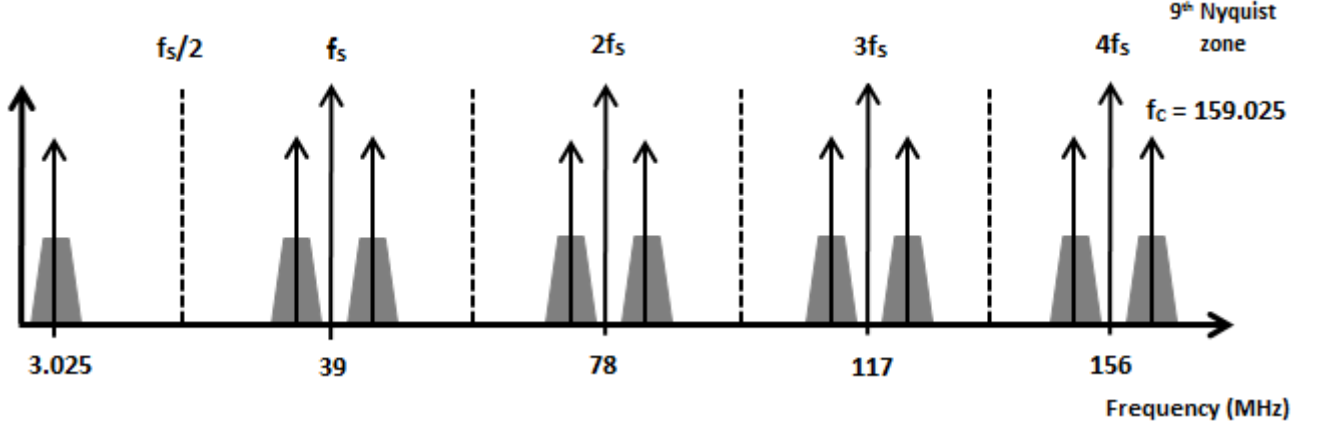


Figure 3.3: 39MHz sample rate to capture the maritime bandwidth in the 9th Nyquist zone.

interest (AIS channels 1 or 2) uses only 25kHz. By oversampling an AIS channel with a sample rate of 39MHz the processing gain can be estimated as follows:

$$SNR_{Process\ gain} = 10\log\left(\frac{39MHz/2}{25kHz}\right) = 29dB \quad (3.1)$$

Therefore, an additional 29dB of process gain can be added to the captured signal. This is a significant improvement to the SNR. However, it must be noted that the process gain only represents the improvement in channel noise floor not the signal level. Lowering the channel noise floor in the digital domain directly improves the sensitivity of the receiver. To achieve the targeted receiver sensitivity of -113dBm, it is important to maintain the noise floor as low as possible, so that weak digitized signals do not get lost in the noise floor. The receiver SNR is ultimately determined by the characteristics of the ADC used in the front-end. The next section will focus on the selection of an ADC to captures the aliased components by implementing the frequency strategy plan that has been developed.

3.1.2 ADC Selection for Direct Digitization

The ADC used in the front-end must acquire a full-power bandwidth much higher than the Nyquist bandwidth ($f_s/2$) to successfully alias the desire bandwidth from higher frequencies [58]. For example, it is not unusual to find a 1GHz full power bandwidth on a 100MHz sampling ADC [59]. This characteristic allows the ADC to subsample bandpass signals centred at frequencies higher than $f_s/2$. However, at higher input frequencies, the ADC becomes slew-rate limited. It

is recommended to keep the centre frequency of the bandpass signal to no more than 10% to 30% of the ADC's full-power bandwidth, depending on the performance of the ADC [59]. As was shown in Figure 3.3, using a high sample rate allows the use of a lower Nyquist zone to alias the signal. This typically will reduce the full-power bandwidth requirements, and minimize the risk of exceeding slew-rate limitations. An ADC to subsample the maritime bandwidth would ideally have a full power bandwidth greater than 536.75MHz (30% of 536.75MHz equals 162.025MHz) so that the maritime bandwidth does not exceed the ADC's slew-rate.

Generally, when selecting an ADC, as speed goes up, the resolution of the ADC goes down [45]. High sample rates allow more bandwidth, but higher resolution allows more dynamic range. This is one of the principle trade-offs in ADC selection. To directly digitization a wide bandwidth, the ADC must have the capability to handle all signals captured, good or bad. The digitized maritime bandwidth is likely to include strong interfering signals as well as weaker signals of interest. To distinguish the two signals, the ADC must maintain the dynamic range imposed by the blocking requirements, which is given in Table 2.1.

To achieve the blocking requirements set in IEC 62278-1, the receiver must successfully receive a wanted signal at -101dBm in the presence of a blocker at -23dBm or -15dBm. Under test conditions the -23dBm blocker is centred at $\pm 500\text{kHz}$, $\pm 1\text{MHz}$ or $\pm 2\text{MHz}$ from the carrier, and the -15dBm blocker is centred at $\pm 5\text{MHz}$ or $\pm 10\text{MHz}$ [1]. Therefore, the required dynamic range corresponding to the difference in signal levels is 78dBc for -23dBm blockers and 86dBc for -15dBm blockers. The location of the blocker in relation to the wanted signal is of great importance when testing the dynamic range. The closer the blocker lies to the wanted signal the more likely the wanted signal gets lost in the signal power of the blocker [60]. From these requirements we can begin determining the ADC necessary to accomplish a direct digitization receiver that complies with the IEC specifications.

ADC datasheets denote the dynamic range as SFDR. ADC's that can achieve an SFDR of 86dBc will typically have a resolution of ≥ 14 bits and have a sample rate of $\geq 170\text{MHz}$. Table 3.1 displays the ADC's on the market from some of the leading ADC manufactures: Texas Instruments (TI), Analog Devices Inc. (ADI) and Linear Technology. The range of ADC devices shown, detail the differences in performance parameters. The ADC's shown in Table 3.1 vary in resolution from 10 to 16 bits, and sample rates from 20MHz to 200MHz. The only ADC's

Manufacturer	Device	Resolution (bits)	Data rate (MSps)	SNR (dBFS)	SFDR (dBc)	Power BW (MHz)	Supply (V)	Power (mW)	Price USD (\$/1k)
TI	ADC12040	12	40	70	84	100	5	340	8.55
	ADC12020	12	20	70	84	100	5	185	6.49
	ADS805	12	20	68	74	270	6	300	9.9
	ADC14L020	14	20	74	93	150	3.3	150	12
	ADC14L040	14	40	74	90	150	3.3	235	15.3
ADI	AD9609	10	20/40/65/80	61	73	700	1.8	45.2/54.7/67.7/76.3	3.5/3.75/4.17/4.5
	AD9629	12	20/40/65/80	69	83	700	1.8	45/56.7/81.7/93	5.25/6.85/12.08/16.70
	AD9235	12	20/40/65	69	84/85/80.5	500	3	90/165/300	7.08/7.99/12.14
	AD9649	14	20/40/65/80	71.5	80	700	1.8	45.2/57.2/75.2/86.8	12/15.13/23.35/25
	AD9245	14	20/40/65/80	71	84/85/80.5/79	500	3	90/165/300/366	11.01/15.92/23.23/31.37
	AD9683	14	170	70.6	89	1000	1.8	365	38.4
	AD9467	16	200	75.6	95	900	1.8	536	100.3
Linear	LTC2226/27/28	12	25/40/65	71.3	80	575	3	75/120/205	7.5/9.17/14.16
	LTC2256	12	25/40/65	70.4	84	800	1.8	34/47/79	11.45/12.05/17.1
	LTC2246/47/48	14	25/40/65	73.3	80	575	3	75/120/205	14.23/18.8/27.69
	LTC2256	14	25/40/65	72.6	84	800	1.8	35/49/81	17.61/21.68/30.78
	LTC2160/61/62	16	25/40/65	76.2	84	550	1.8	45/63/87	30.36/36.43/46.54

Table 3.1: A list of ADCs from TI, ADI and Linear Technologies.

that achieve a SFDR > 86dBc are the AD9623 and the AD9467. The cost of these ADC's are well above budget. Initially, Vesper Marine would like to target an ADC of $\leq \$10$. The ADC's shown in Table 3.1 of this price range are the 10 or 12 bit ADC's. Another important parameter to consider is the ADC's full power bandwidth. The ADC's that acquire a power bandwidth of > 536.75MHz also limits our choice.

In Figure 3.3, the sample rate used to successfully subsample the maritime bandwidth was 39MHz. Therefore, a 40MSps (mega samples per second) ADC would be ideal. The research on ADC devices concluded that the AD9629 40MHz [61] fits all the requirements for the direct digitization receiver, apart from its SFDR rating of 83dBc, falling 3dB short of the blocker requirement. However, extra gain from post-processing in the digital domain may help improve the receiver's dynamic range, this will be investigated later in Chapter 5. Implementation of subsampling should not be an issue for the AD9629, as the maritime bandwidth lies at 23% of its full power bandwidth of 700MHz. The AD9629 also has one of the lowest power ratings in Table 3.1, accomplishing 56.7mA with a 1.8V supply.

One of the most important parameters is the AD9629's full scale SNR (SNRFS). With a SNR = 69dBFS, the AD9629's channel noise floor is 69dB below the full scale power. The AD9629 has full scale power of +10dBm, as a result the channel noise floor lies at -59dBm. Therefore, signals at the ADC's input above -59dBm will successfully be digitized. However, as discussed in Section 3.1.1 oversampling the AIS signal at a rate of 39MHz can achieve a process gain of 29dB. By adding the gain achieved from post-processing to the rated SNR of the AD9629, the theoretical SNR of the channel is 98dBFS. Figure 3.4 illustrates the resulting noise floor levels from oversampling the AIS channel bandwidth (25kHz). The full scale power (i.e. signal power before saturation) of the AD9629 is +10dBm. Hence, the channel noise floor after post-processing is +10dBm - 98dBFS = -88dBm. The ADC noise floor over the Nyquist bandwidth (19.5MHz) is -132dBm, then selecting the channel with a bandwidth of 25kHz, the noise floor increases to -88dBm. Through post-processing the digitized bandwidth, signals above -88dBm should theoretically be successfully converted to the digital domain.

From Figure 3.4, it is also possible to determine the noise figure of the ADC [62, 63]. Equation (2.10) shows an expression for the ADC noise figure, this equation corresponds to the noise floor levels in Figure 3.4. Because we know that the thermal noise power is equal to -174dBm (at

room temperature) the ADC noise figure, NF_{ADC} can be found:

$$NF_{ADC} = 10dBm + 174dBm - 69dBFS - 10\log_{10}(19.5MHz) = 42dB \quad (3.2)$$

Therefore, the ADC noise figure, NF_{ADC} is 42dB. As discussed in Section 2.4.1, noise figure gives designers an indication of the components necessary in the AFE to maintain a low system noise figure [43]. Managing the system noise figure, NF_{sys} will be discussed further in Section 3.3.2.

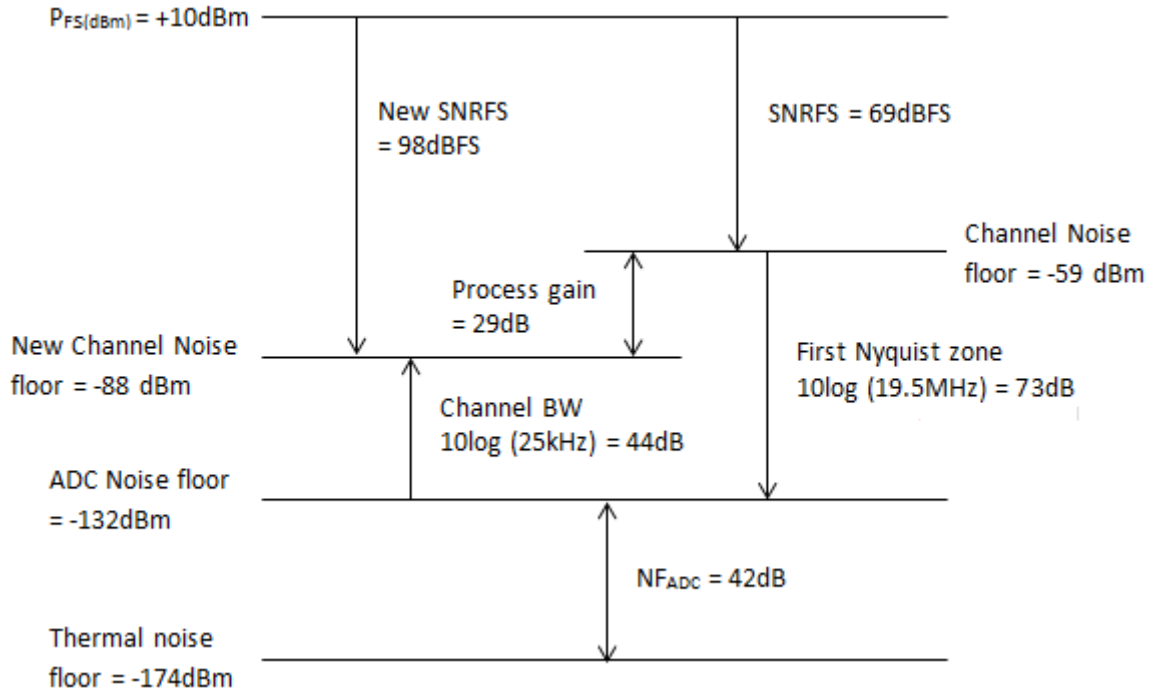


Figure 3.4: Resulting noise floor levels from implementing oversampling.

3.2 HIGH SPEED DATA EVALUATION

To support the evaluation of AD9629 with real-time data, the AD9629 evaluation board [61], and data capture board [64] shown in Figure 3.5 was purchased from Analog Devices. This platform allows users to observe the AD9629 capability to digitize an input signal via PC. Software known as VisualAnalog is used to aid the analysis of the sampled data. There are a number of test methods that can be conducted in both the time and frequency domain using VisualAnalog. These provide performance measures of the digitized signal in real-time, allowing designers to investigate frequency planning strategies. This section will apply AIS signals to the evaluation kit

with the aim of investigating the AD9629's ability to subsample maritime signals. As discussed in Section 3.1.2, we are interested in aliasing the maritime bandwidth from the 9th Nyquist zone using a sample rate of 39MHz. FFT test results of the Nyquist bandwidth will be collected to observe the aliased components. This process will validate the signal quality of the aliased signals and the frequency plan illustrated in Figure 3.3.

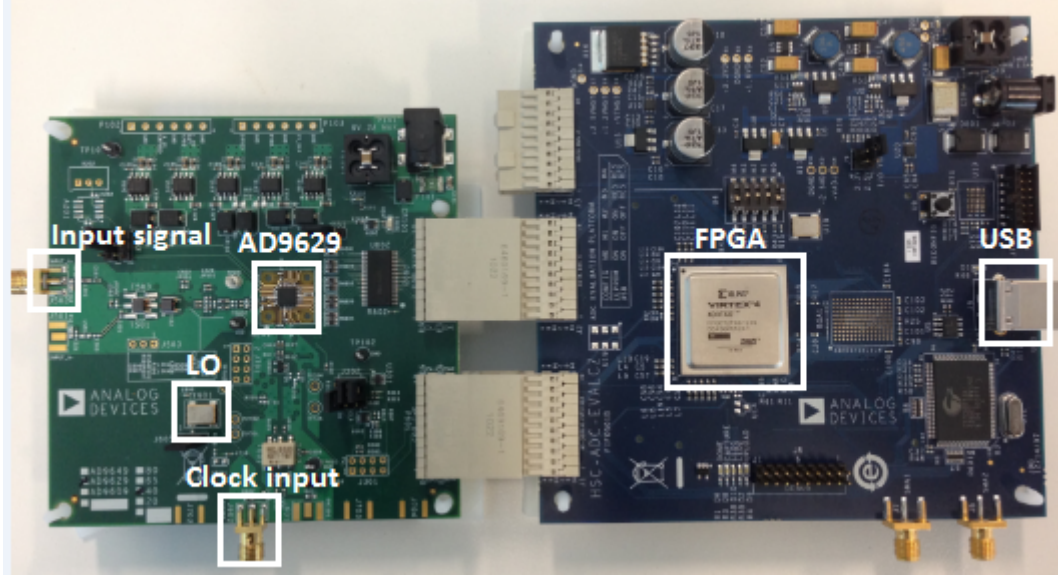


Figure 3.5: ADC evaluation board (left) and the data capture board (right).

3.2.1 Implementing the Frequency Planning Strategy

Tests are conducted by feeding an AIS signal into the input connector of the ADC evaluation board and observing the digitized data gathered by the data capture board using VisualAnalog. Following the signal chain from left to right in Figure 3.5, the incoming signal gets sampled by a reference clock from the on-board LO or an input clock source. The AD9629 outputs the sampled data via a 12-bit parallel port interface (PPI), that gets fed into the data capture board. Two connectors shown in Figure 3.5 are used to interface data and serial peripheral interface (SPI) capabilities between the two boards. The USB interface from the data capture board streams the data captured in the FPGA to the PC, allowing the data to be displayed and measured [65]. Data formatting is accomplished over SPI. For all test the output data is formatted as two's complement.

Before feeding the input signal into the ADC evaluation board, anti-aliasing filtering must

be implemented. The SAW filters utilized on Vesper's Mimosa board are used to band-pass filter the maritime bandwidth. The input signal fed into the ADC evaluation board is AIS channel one, which has a carrier frequency of 161.975MHz. To investigate the aliased components, VisualAnalog was used to capture a FFT of the Nyquist bandwidth, this is shown in Figure 3.6. It is clear that the carrier at 161.975MHz was successfully aliased to 5.975MHz, as was illustrated in Figure 3.3. The location of the subsampled carrier is denoted in the left column as the Fund Frequency. The measured full scale SNR is 69.577dBFS, which meets the rated SNR on the AD96929 datasheet of 69dBFS [61]. It is important to note that the full scale power is referenced from 0dBm in Figure 3.6 not +10dBm. The measured SNR corresponds to the Average Bin Noise, the FFT sample size adds process gain to the SNR, lowering the noise floor, which is represented by the Average Bin Noise parameter. For the test shown in Figure 3.6 a bin size of 16384 is used. Therefore, the FFT process gain can be calculated using the follow equation [66]:

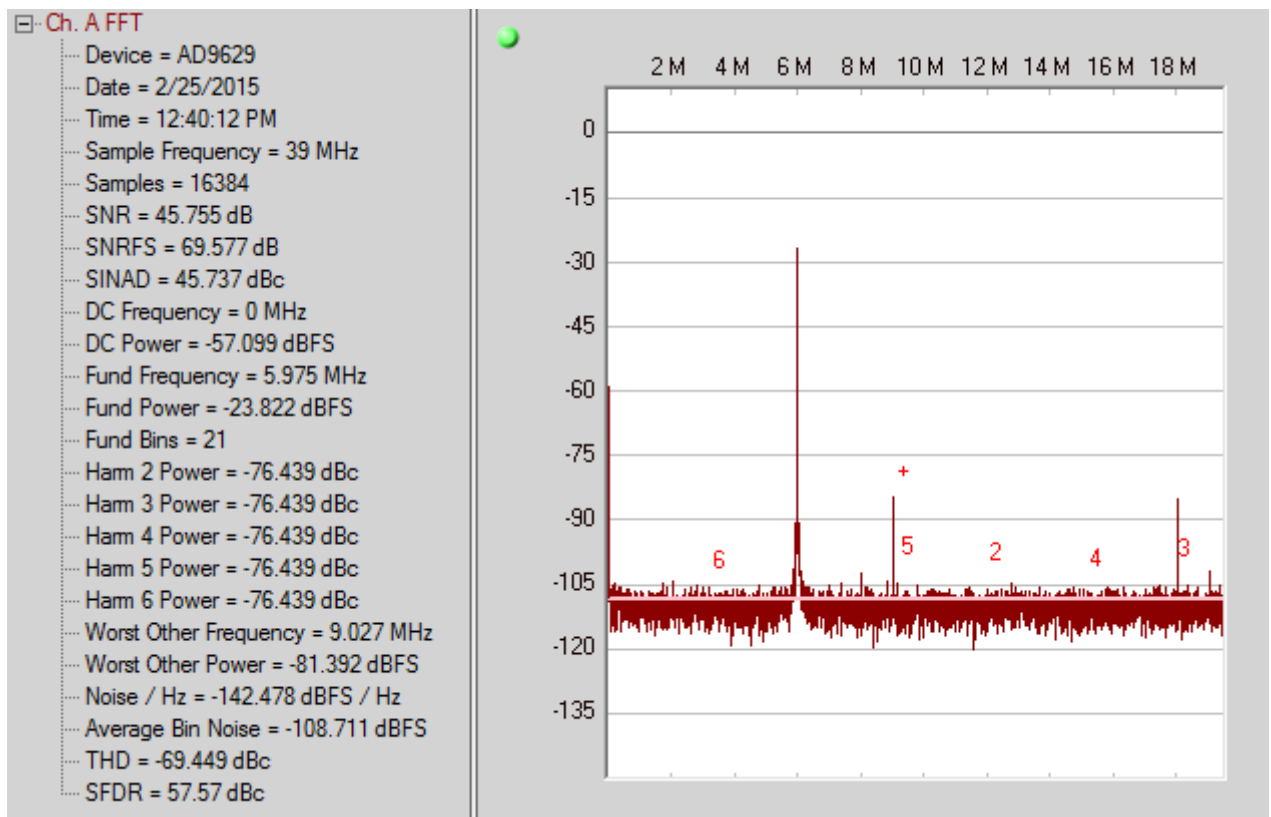


Figure 3.6: An FFT of the Nyquist bandwidth using a sample rate of 39MHz. This demonstrates the AIS signal at 161.975MHz getting subsampled to 5.975MHz.

$$FFT_{process\ gain} = 10\log\left(\frac{M}{2}\right) \quad (3.3)$$

Where M is the sample size of the FFT. Using a bin size of 16384 gives a process gain of $FFT_{process\ gain} = 39.134dB$. By subtracting $FFT_{process\ gain}$ from the Average Bin Noise of -108.711dBFS the full scale SNR is found, $SNR=69.577dBFS$. Increasing the FFT's sample size to represent the signals in the Nyquist bandwidth reduces the noise floor, which is similar to the process gain obtained from oversampling. Therefore, signals below the ADC's rated SNRFS can be observed.

The measurements taken with respect to full scale power provide the computation for the ADC's sensitivity. However, it is also very useful to observe measurements with respect to the carrier signal level. The SNR and SFDR measurements, shown in Figure 3.6, are taken with respect to the Fund Power measure of the carrier, in units of dBc. The measured $SNR=45.755dBc$, is given by the difference between full scale SNR and the Fund Power of the carrier signal (-23.822dBFS). Similarly, the measured $SFDR=57.57dBc$, is given by the range between the Worst Other Power (-81.392dBFS) and the Fund Power. This provides a good indication of the digitized signal quality. From this analysis we can see that the aliased carrier signal is 45.755dB above the noise, and the range between the carrier signal strength and the worst spurious is 57.57dBc.

The Worst Other Power is located at 9.027MHz, this harmonic appears to be a product of the signal generated at the input connector and the LO. At 18.023MHz there is also a harmonic with a similar signal strength. It must be noted that these are not the 3rd and 5th harmonics calculated by VisualAnalog, but purely a result of the input signals. By observation these harmonics lie outside the aliased maritime bandwidth, which is now encompasses 25kHz to 6.025kHz. Therefore, they will not interfere with AIS signals, and can be removed by digital filtering via post-processing to improve the measured SNR.

The measured Worst Other Power equals -81.392dBFS, therefore, increasing the carrier signal level to fullscale should result in a SFDR close to -81.392dBc. Figure 3.7 shows the same test but the carrier signal level is increased to just below full scale power. The measured SFDR has not been affected, and still remains at 57.742dBc. As shown Figure 3.7, the Worst Other Frequency is now measured at 18.023MHz. As the signal level is increased, the Worst Other Power has also increased, measuring -62.579dBFS. Therefore, the SFDR remains at 57.742dBc. An interesting

observation is the measured harmonic numbers in both Figure 3.6 and Figure 3.7 remain at the same level. Datasheets typically measure the SFDR with respect to the second or third harmonic [41]. Hence, the SFDR with respect to the second and third harmonics is -76.439dBc. Therefore, the rated SFDR=83dBc of the AD9629 is not quite met.

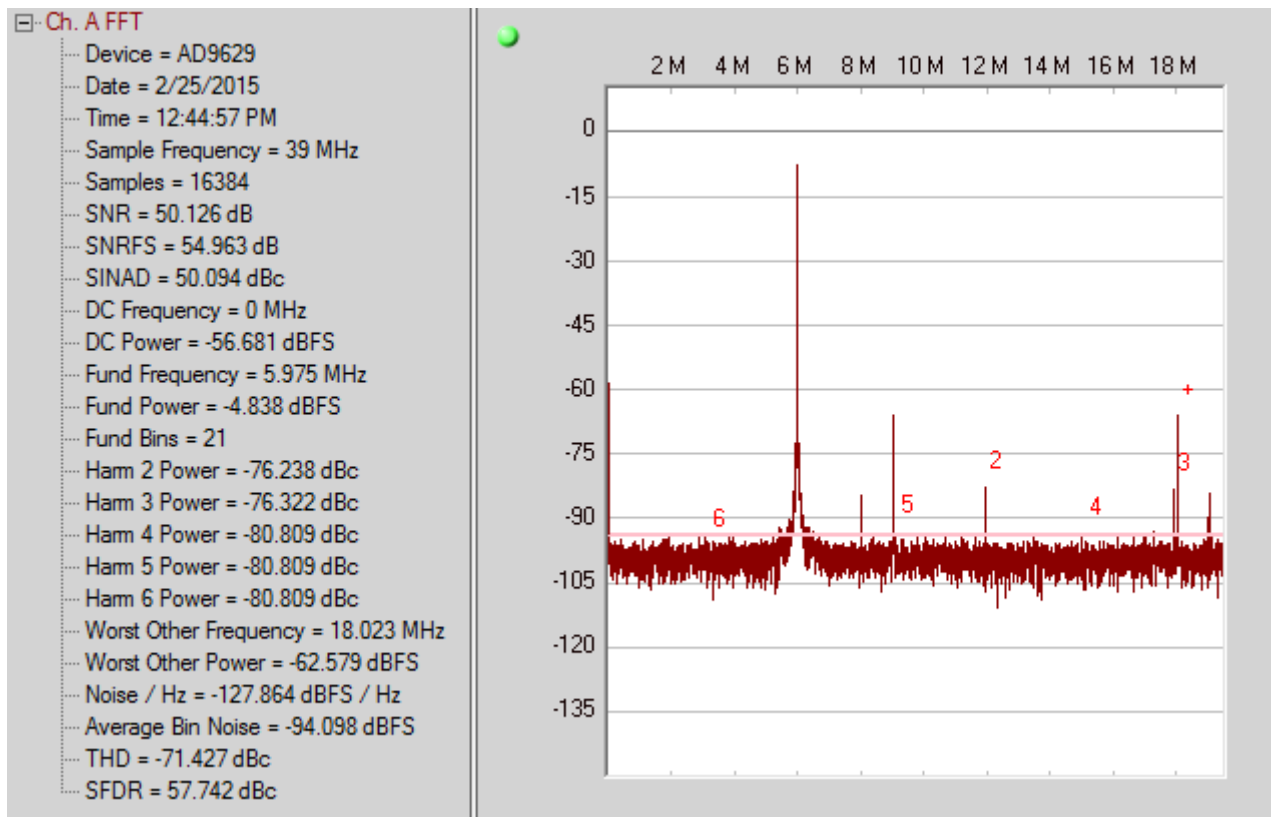


Figure 3.7: An FFT demonstrating the increase in noise when the input signal level is increased just below full scale power.

The increase in signal level also seems to reduce the ADC's SNR performance. As shown in Figure 3.7 the full scale SNR is now 54.963dBFS, diminishing 14.589dB from the full scale SNR measured in Figure 3.6. The noise power from the signal generators seem to over power the ADC noise, decreasing the measurements referenced from full scale power. As signal level is increased at the signal generator the phase noise about the carrier signal becomes more noticeable. The HP8920A RF communications test set used to conduct these tests has a phase noise of <-110dBc/Hz at 1GHz with 20kHz offset [67]. Therefore, the generated signal will introduce added noise to the measured results.

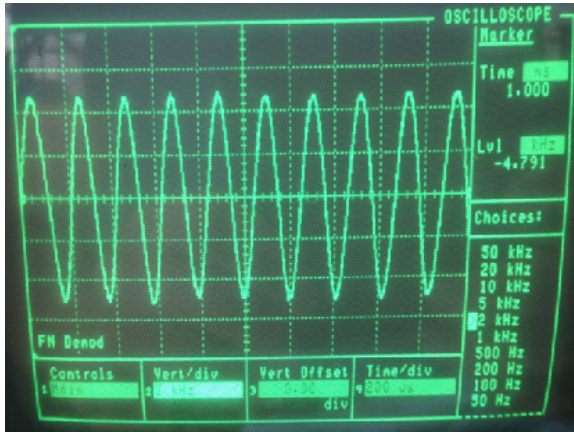
From the high speed data analysis we can conclude that the aliased representation of AIS

signal was successfully captured by the AD9629 subsampling at 39MHz, this analysis verified the frequency planning strategy shown in Figure 3.3. However, the rated SFDR and SNR was not met when the carrier power was increased to just below full scale. The full scale SNR shown in Figure 3.7 was measured at 54.963dBFS. Although, in Figure 3.6 the full scale SNR=69.577dBFS, matching the rated value. In this case the signal power was only -23.822dBm. By lowering the signal power from the signal generator the effect of phase noise becomes less pronounced. The receiver performance will rely heavily on the digital receiver signal chain to improve the receiver's SNR, and thus it's sensitivity. Implementation of the DDC will identify if the aliased AIS signal captured in the Nyquist bandwidth has acquires the signal integrity to perform baseband processing.

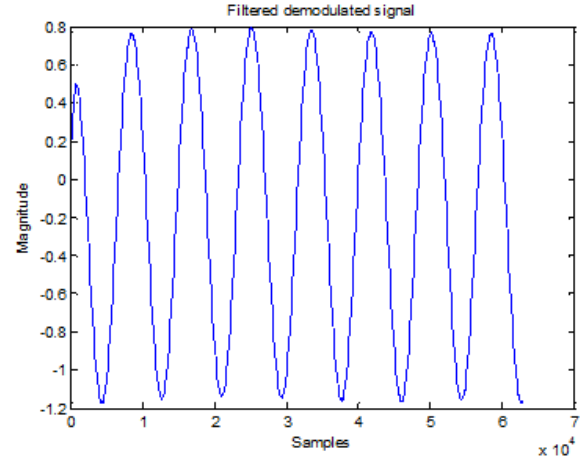
3.2.2 FM Demodulation using MATLAB

To analyse the subsampled signal further, the data captured in the FFTs can be exported by VisualAnalog into MATLAB to conduct digital signal processing algorithms. Using the subsampled data collected by the data capture board, a simulation of FM demodulation was accomplished. The AIS test signal fed into the ADC evaluation board is generated from the Mimosa board. Vesper Marine's AIS software provided the capability to program the Mimosa to transmit an AIS test signal. There are five different AIS test signals used for IEC test methods, which are detailed in IEC 62287-1 [1]. By receiving either one of these test signals, an evaluation of the AIS audio signal can be conducted. This section describes an implementation of FM demodulation on the subsampled AIS test signal.

The MATLAB code imports an Excel spread sheet, which contains the 12-bit data captured in VisualAnalog, and simulates the filtering and demodulation process on the digitized signal. On AIS channel one (161.975MHz), AIS test signal number two is fed into the ADC evaluation board, which consist of a series of 1's and 0's as the data [1]. As a sanity check, the HP8920A is also used to observe the AIS audio signal by executing it's own FM demodulation function. It must be noted that for this test the AIS test signal was fed directly into the HP8920A without any subsampling. Figure 3.8 provides a comparison of the AIS audio signal demodulated from the AIS test signal. The waveforms produced by the two different tests show identical signals, both showing a series of 1's and 0's at a frequency of approximately 5kHz. The sample size used



(a) Audio data demodulated using the HP8920A RF communications test set.

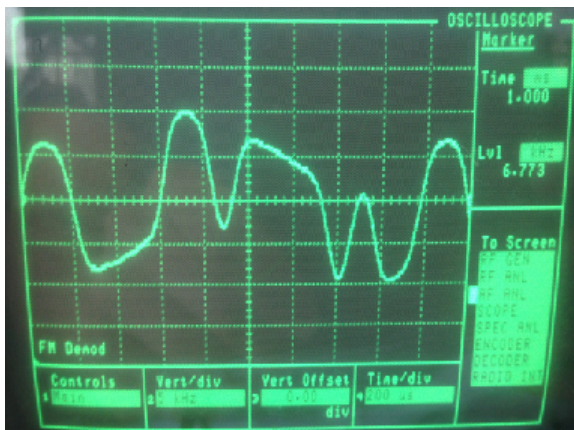


(b) Audio data demodulated using MATLAB.

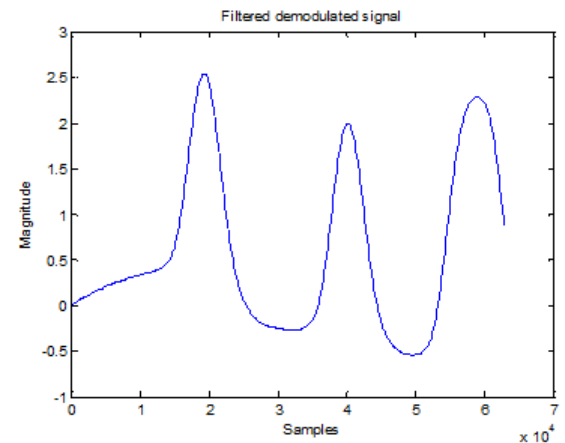
Figure 3.8: FM demodulation of test signal number two.

(shown on the x-axis) in Figure 3.8b was increased from 16384 to 65536, providing more data to represent on the plot. The waveform shown in Figure 3.8b has a transient response for the first few samples, resulting from the FIR filters used in the code. Overall, the comparison shown in Figure 3.8 confirms the message signal is preserved throughout the subsampling process.

Using the same test method, AIS test signal four was fed into both the HO8920A and ADC evaluation board. The audio signal used on test signal four is pseudo random 1's and 0's. Figure 3.9 shows the demodulated waveforms, both displaying pseudo random data. Figure 3.9a and Figure 3.9b do not display the same waveform because of the pseudo random characteristics.



(a) Pseudo random data demodulated using the RF communications test set.



(b) Pseudo random data demodulated using MATLAB.

Figure 3.9: FM demodulation of test signal number four.

The analysis from both Figure 3.8 and Figure 3.9 verified the AD9629 used to subsample the AIS channel preserved the AIS audio signal.

As discussed in Section 1.3.3, a DSP will be investigated to implement the FM demodulation on the AIS signal in real-time. The quality of the AIS audio signal from the DSP will ultimately determine if the receiver signal chain has accomplished the necessary performance to up hold the targeted sensitivity. As was shown in Figure 1.1, the FM demodulated signal is passed into the CMX7032 to execute the AIS baseband processing that produces the VDM data. This will be explored in Chapter 5.

3.3 ANALOG FRONT-END REQUIREMENTS

To achieve the ADC's performance measurements taken in Section 3.2, implementation of the AD9629 must be designed hand-in-hand with the analog stages preceding it. If the AFE signal chain is poorly designed then signals fed into the AD9629 will not achieve the optimal SNR in the digital domain [36]. This section will look at the design requirements for implementing the filter and amplifier stages for the direct digitization receiver. The existing Mimosa board already employs it's own AFE stages, as was shown in Figure 1.1. For a cost effective approach, the signal chain designs for the SDR will investigate the components used on the Mimosa board and attempt to implement them in the AFE. To determine if the components are suitable for the AFE design, calculations of the noise figure and required gain will be analysed. This analysis will refer back to the targeted sensitivity and IEC receiver standard [1].

3.3.1 Amplifier and Filter Stages

As discussed in Section 1.3.1, the SDR is band-limited to the VHF maritime band from 156.025MHz to 162.025MHz. Therefore, all signal processing in the AFE is fixed on the these frequencies. This characteristic does not change from the existing front-end on Mimosa board preceding the IF stage, as shown in Figure 1.1. Therefore, it make sense to employ the existing SAW filters, which are the MA06510 [68]. Note that these are the same band-pass filters (BPF) used for anti-aliasing.

Typically, filters are applied directly after the antenna in the signal chain, and before any amplification is injected. This is so that out-of-band signals are attenuated before they enter

the amplifier. It is good practice to use BPFs after the amplifier as well so that no out-of-band signals are amplified and fed into the ADC. In Section 3.1.2, the calculated channel noise floor after post-processing is -88dBm. Relating the channel noise floor to the targeted sensitivity of -113dBm, a gain of >25dB is required to amplify -113dBm signals above the channel noise floor. However, it is also important that the desired signal is not amplified to signal levels above the AD9629's full scale power (+10dBm), causing the ADC to saturate. For wideband SDR receiver design, an automatic gain controller (AGC) is typically included. The applied gain by an AGC corresponds to the feedback on the signal levels seen by the ADC. Therefore, the gain can be adjusted to maintain signal levels below full scale power and above the noise floor [69].

The amplifier used on the Mimosa board is the BGA614 [70], which is a LNA capable of 19.5dB of gain. A single BGA614 amplifier will not achieve the -113dBm sensitivity, therefore, two LNAs will be implemented in the AFE. The total gain injected will be up to 39dB. However, the receiver specification in Table 2.1 states that signals at high input levels, up to -7dBm must result in 10% PER. The caveat with this is applying 39dB gain to -7dBm signals will saturate the ADC, clipping the input waveform. Taking a closer look at the datasheet of the BGA614, it was found that the applied gain corresponds to the device current, I_D , the gain to device current characteristic is shown in Figure 3.10. By varying the device current, the LNA can act as an AGC. Although, AGC functionality relies on the feedback loop to adjust the gain accordingly. A possible solution is to use a bank of switched resistors, each used to apply a different device current to the BGA614. Figure 3.11 show the general circuitry of the BGA614. Changing the bias resistor value, R_{bias} can dictate the device current, I_D . To switch between resistor values, a feedback path from a programmable device can be used that changes what resistance to apply, which will correspond an adjustment in the applied gain.

The AFE prototype will use three different resistor values to change the device current of the BGA614. Using Figure 3.10 the gain can range from approximately 10dB to 19dB. The gain levels chosen are:

- 10dB - device current of 10mA with $R_{Bias} = 201\Omega$.
- 16dB - device current of 15mA with $R_{Bias} = 184\Omega$.
- 19dB - device current of 50mA with $R_{Bias} = 67\Omega$.

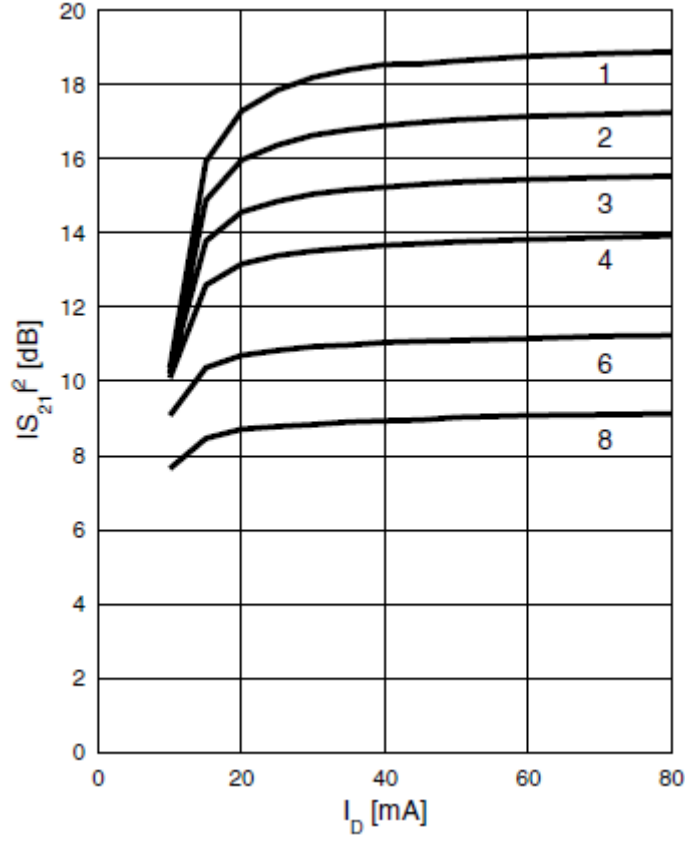


Figure 3.10: Graph showing the variation in gain, $IS_{21}I^2$ of the BGA614 with respect to the device current, I_D . Eight plots are shown representing the input frequency from 1GHz to 8GHz, in increment steps of 1GHz [70].

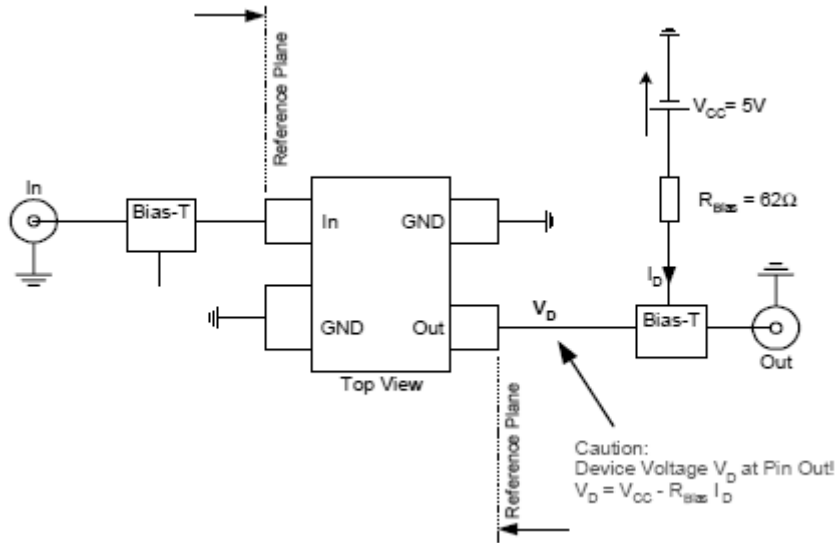


Figure 3.11: General description of the BGA614 circuitry. The device current, I_D can be changed by using different resistor values at R_{bias} [70].

Applying this method of AGC to both LNAs in the AFE, a gain range of 20dB to 38dB can be accomplished. Keeping the BGA614 in Vesper's AIS products will benefit the BOM of the SDR. There are AGC devices on the market suitable the AFE, such the AD8370 [71], which is a digitally controlled variable gain amplifier (VGA). However, the AD8370 costs \$4.91 (USD per 1k) [72], whereas the BGA614 only costs \$0.95 (NZD per 3k) [73]. The AFE prototype will incorporate an AGC stage using the BGA614 for future evaluation purposes. AGC functionality will not be investigated in this project, but will be incorporated in the AFE prototype for future performance analysis.

3.3.2 Cascaded Noise Figure

Throughout the AFE signal chain, each device up to, and including the ADC, will contribute to the receiver's system noise figure, NF_{sys} . To reiterate, the NF of a device is the degradation in SNR as a signal passes through it [74]. The concept of NF_{sys} characterizes the fundamental limitation of the receiver's sensitivity. Designing the AFE using cascaded amplifiers (in this case two BGA614s) means that at each stage the in-band signal(s) and noise get amplified. As discussed in the previous section, the filtering stages are implemented before and after each amplifier stage so that out-of-band signals are suppressed. Figure 3.12 shows the consecutive BPF and LNA stages used to condition the incoming signal in the AFE.

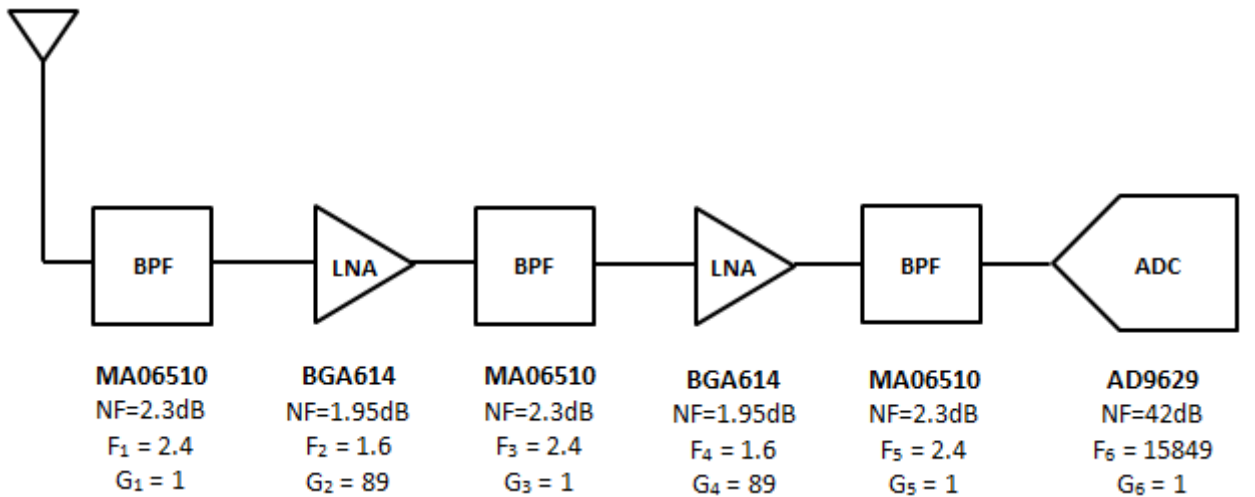


Figure 3.12: Amplifier and filter stages in the analog front-end signal chain. Illustrating the noise figure, NF in dB and the noise factor, F and gain, G in linear units.

To investigate the implications of NF on the receiver, Friis's equation for cascaded noise figure stages is used [43, 74], shown in the following equation:

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \frac{F_4 - 1}{G_1 \cdot G_2 \cdot G_3} + \dots \quad (3.4)$$

This section will not go through the deviation of Friis's equation as it is described thoroughly in [75]. To calculate NF_{sys} the noise figure and gain of each component in the signal chain must be converted from dB to linear units. Friis's equation calculates the system noise factor, F_{sys} , which is the linear unit for NF i.e. $NF = 10\log(F)$. It can be seen from Equation (3.4) that the first stage in the signal chain dominates the system noise factor, F_{sys} . Furthermore, the gain applied in the first stage reduces the contribution of noise factor in the following stages [43]. As shown in Figure 3.12, the noise factor, F and gain, G for each component have been converted to a linear scale, so the values can be substituted into Equation (3.4). From the cascade stages in Figure 3.12 the calculated system noise factor, F_{sys} is:

$$F_{sys} = 2.4 + \frac{1.6 - 1}{1} + \frac{2.4 - 1}{1 \cdot 89} + \frac{1.6 - 1}{1 \cdot 89 \cdot 1} + \frac{2.4 - 1}{1 \cdot 89 \cdot 1 \cdot 89} + \frac{15849 - 1}{1 \cdot 89 \cdot 1 \cdot 89 \cdot 1} = 5.0272 \quad (3.5)$$

Then converting the system noise factor, F_{sys} to noise figure we find:

$$NF_{sys} = 10\log(F_{sys}) = 10\log(5.0272) = 7dB \quad (3.6)$$

Therefore, the noise introduced throughout the AFE signal chain is approximately 7dB. The calculated noise figure of the AD9629 in Section 3.1.2 was $NF_{ADC}=42dB$. By implementing the amplifier and filter stages illustrated in Figure 3.12, the noise contribution of the AD9629 has been significantly reduced. Ideally, the system noise figure throughout the AFE would be as low 3dB for RF applications. However, 7dB is reasonable. Testing the receiver sensitivity of the SDR prototype will dictate the importance of optimizing the cascaded stages in the AFE. Further work to optimize the system noise figure to levels around 3dB will involve investigating the AFE configuration and searching for more suitable components.

3.4 THE FRONT-END PROTOTYPE BOARD

Development of the front-end prototype board began with the question: what capabilities does the prototype need to afford? Building the prototype not only needs to complete the SDR architecture described in Section 1.3, but also provide the flexibility to modify and test certain methods that are, or may need to be, implemented on the board. The general structure and components used for the AFE have been described. The idea for the AFE prototype board is to provide an interface between the AD9629 output data and evaluation boards for the FPGA and DSP, carrying out the receiver structure introduced in Section 1.3.2 and Section 1.3.3. Implementation of programmable devices will be presented in the next chapter. For now, the discussion focuses on the development of the AFE.

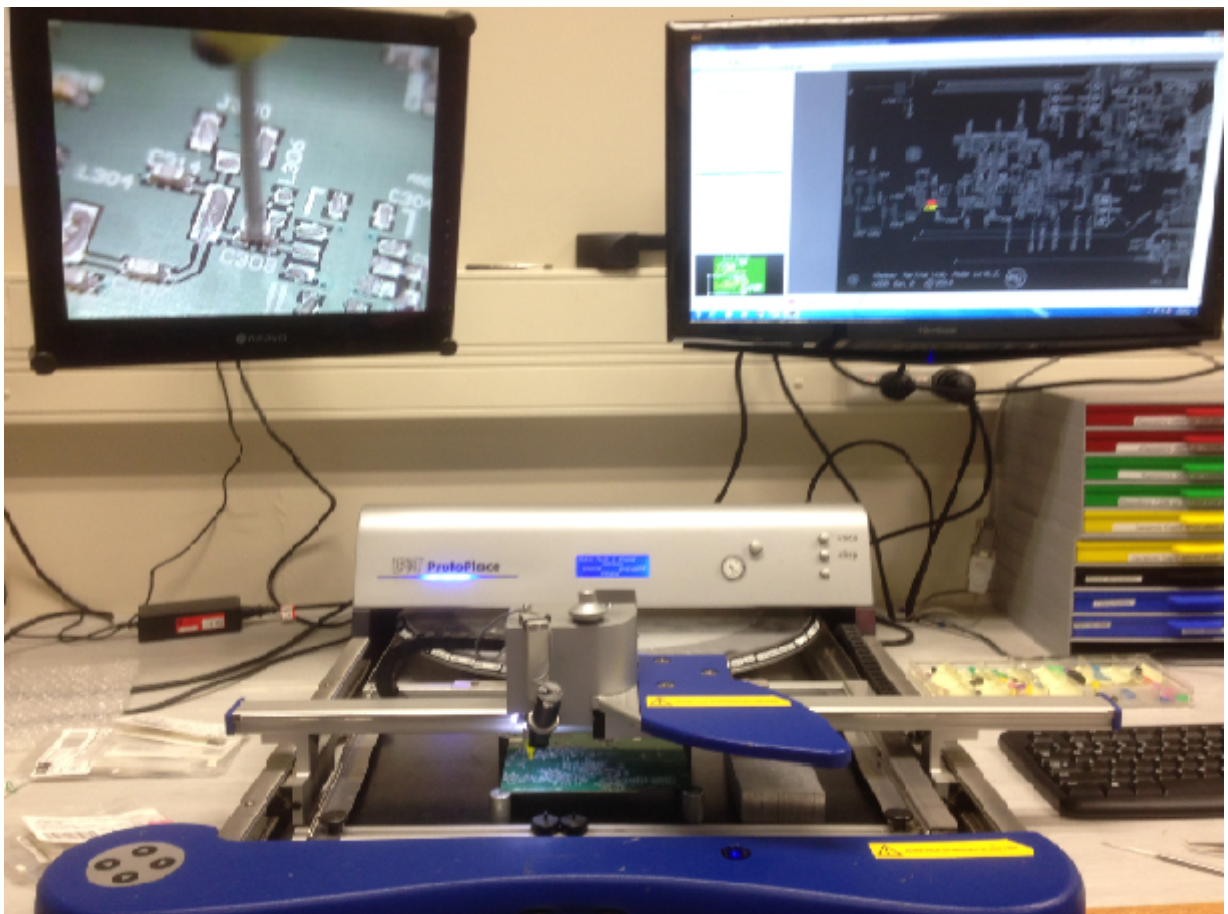


Figure 3.13: The component placement machine used to load the components on the front-end prototype board.

The evaluation of the front-end prototype board using the data capture board is of significant importance, so that the earlier results in Section 3.2 can be compared. With this in mind, the ADC evaluation board used with the data capture board is used as a template to analyse the 12-bit data. Essentially, the AFE prototype board will replace the ADC evaluation board, shown in Figure 3.5, and use the data and SPI connectors to interface with the data capture board. This will allow the use of VisualAnalog to evaluate the AD9629 output data on the prototype board. The schematic and PCB design of the front-end prototype was developed by Dave Kearney, an RF engineer at Vesper Marine and Carl Omundsen, co-founder of Vesper Marine. Work was completed with Dave and Carl at Vesper over a four month period. Once the PCB for the front-end prototype was completed the board was loaded using the component placement machine shown in Figure 3.13 at the University of Canterbury.

3.4.1 Structure of the Analog Front-End

The signal chain illustrated in the Figure 3.12 can be depicted in Figure 3.14. At each filter stage an IPEX connector is used to afford signal level and filter testing throughout the signal chain. The three resistors corresponding to different gain values, as discussed in Section 3.3.1 are constructed in the first gain stage. The AGC will not be implemented, instead the gain value of the LNA will be set to maximum (i.e. 19.5dB). The AD9629 uses a differential input, which is configured using a double balun transformer. The transformer is a noiseless component, hence the reason why it was not discussed in the signal chain analysis in Section 3.3.

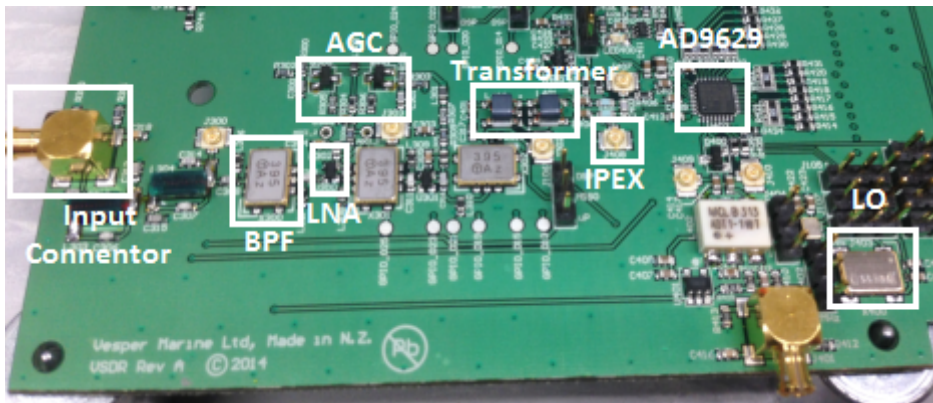


Figure 3.14: Zoomed in picture of the AFE prototype board, detailing the structure of the signal chain.

At the clock source, the prototype board includes two different LOs. The first LO is the RXO2520P [76], which has a frequency of 39MHz and a jitter of 2ps. The second LO is the FXO-HC735-12 [77], this was employed because it is pin compatible with a range of LOs of different frequencies. If a different LO frequency was ever needed for future modifications a simple part swap can be accomplished. There is also the option of using an input clock source via the MCX connector. This option is included for added flexibility for frequency planning. The list of jumpers to the right of the LOs provide the communication capabilities between different devices. Initially, the jumpers are configured for SPI capabilities between the data capture board. The 12-bit data from the AD9629 can be fed to either the data capture board or the FPGA evaluation board, giving us the capability the test signal quality (via data capture board) and also perform digital signal processing in real-time (via programmable devices). The configuration of the interfacing between all boards will be detailed in Chapter 4.

3.4.2 Results Gathered from the Analog Front-End

Before the analog signal becomes digitized, analysis of the signal quality through the signal chain will verify amplifier and anti-alias filtering performance. These tests were conducted using the HP8920A, capable of transmitting and receiving signals to measure the receiver's performance. To test the amplifier and filter stages, an input signal that sweeps frequencies across the maritime bandwidth is fed into the AFE input connector. These frequencies can be measured from the IPEX connectors along the signal chain and displayed via a spectrum analyser. Figure 3.15 shows the filter response at the IPEX connector after the third BPF in the signal chain. Probing through each of the IPEX connectors it was found that both LNAs were injecting a gain of 15dB. Therefore, the total gain from both LNAs is 30dB. The input signal amplitude is -40dBm, by the time the signals reaches the output of the third BPF the signal has an amplitude of -10.48dBm, as displayed in Figure 3.15.

The measured device current, I_D driving both LNAs is 44mA. Referring to Figure 3.10 we should expect a gain of approximately 18.5dB. Therefore, the expected gain from both BGA614s is 37dB (each applying a gain of 18.5dB). However, there seems to be a 7dB of lose in the AFE. This could be a result of insertion loss through the three BPFs. The MA0610 datasheet specifies that the SAW's typically introduce an insertion lose of 2.3dB [68]. Using three BPFs means we

can expect an insertion loss of approximately 6.9dB. This could explain the why only 30dB of gain is applied in the AFE.

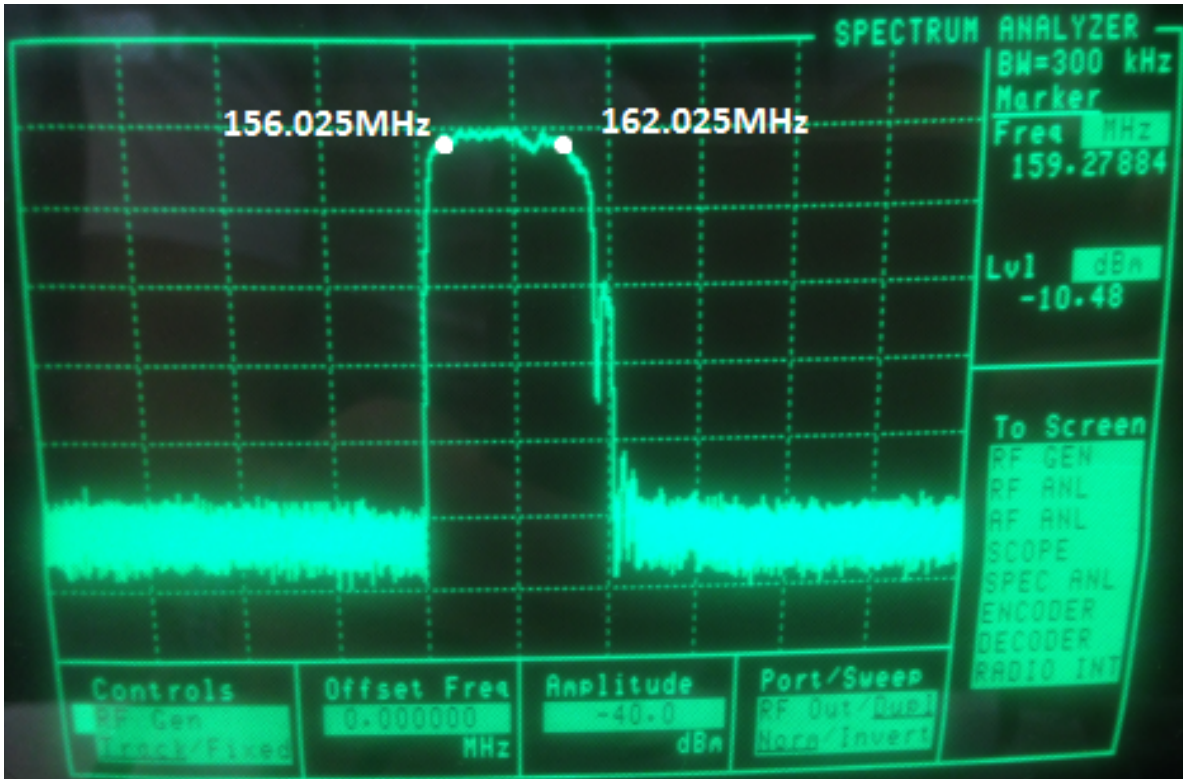


Figure 3.15: Filter response of the MA06510. Frequency sweep of 50MHz with an input signal level of -40dBm. This graph shows a gain of 30dB.

The measured cut-off frequencies of the filter response match the datasheet specifications of the MA06510 [68], displaying a passband from 156.025MHz to 162.025MHz. The cut-off frequency of the MA06510 are obviously not “brick walls”, any signals within the passband of the filter response shown in Figure 3.15 will be fed into the AD9629, and aliased throughout the spectrum. Going back to Figure 3.3, where subsampling the maritime bandwidth using 39MHz was shown, we can picture the filter response in Figure 3.15 as the bandwidth being subsampled. This gives a good indication about what frequency components throughout the spectrum will be aliased.

The digitized data from the AD9629 was fed into the data capture board to display the resulting FFT of the Nyquist bandwidth from the AFE board. The input signal fed into the input connector has a carrier frequency of 161.975MHz (AIS channel one) with an amplitude of -21dBm. Therefore, the signal is just below full scale power when it reaches the ADC input. Figure 3.16 measures the Fund Power at -0.223dBFS. The Fund Frequency shows that the 161.975MHz

carrier has been aliased to 5.975MHz by subsampling at a rate of 39MHz. One interesting measure is the Average Bin Noise, which is relatively high, measured at -86.396dBFS. By observation there seems to be a rise in noise that covers DC to 8MHz in the Nyquist bandwidth. This is the aliased components from the passband of the anti-alias filter (i.e. the passband of the MA06510). Increasing the signal power at the signal generator also seems to increase the noise levels in the passband. The resulting full scale SNR is 47.261dBFS, dropping 22dB below the rated 69dB. Figure 3.17 shows the same signal applied in Figure 3.16 but the signal level at the AFE input connector has been reduced to -94dBm. The resulting Average Bin Noise has decreased from -86.396dBFS to -109.367dBFS, which achieves a full scale SNR of 70.233dBFS, as a result of decreasing the signal level from the HP8920A. As discussed in Section 2.4.2, jitter on the signal can impede the SNR of the ADC. The combination of jitter on both the HP8920A and the LO will result in inaccurate sampled data. Therefore, phase noise about the digitized signal will occur, and will be more profound as the input signal is increased.

In Figure 3.7, the implications of the Worst Other Power measures at 9.027MHz and 18.023MHz

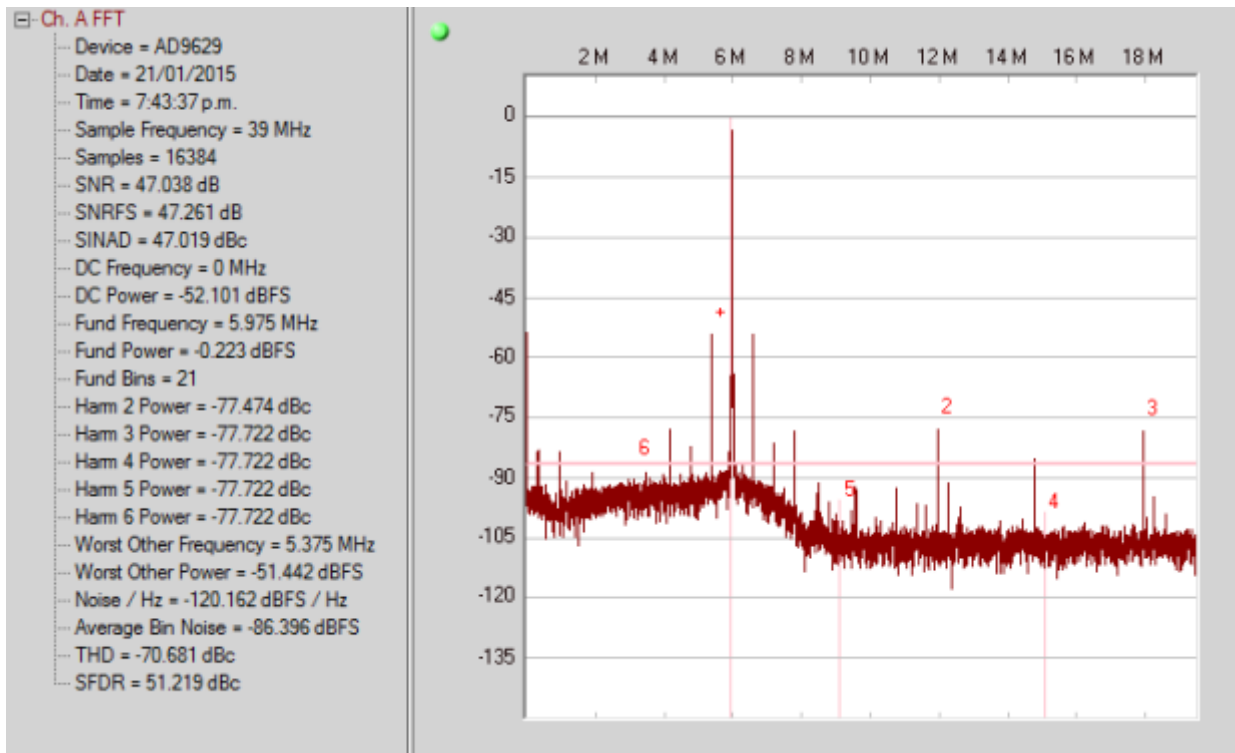


Figure 3.16: FFT of the aliased signal fed into the front-end board. The input signal level was adjusted to -21dBm to get just below full scale power, with carrier frequency at 161.975MHz.

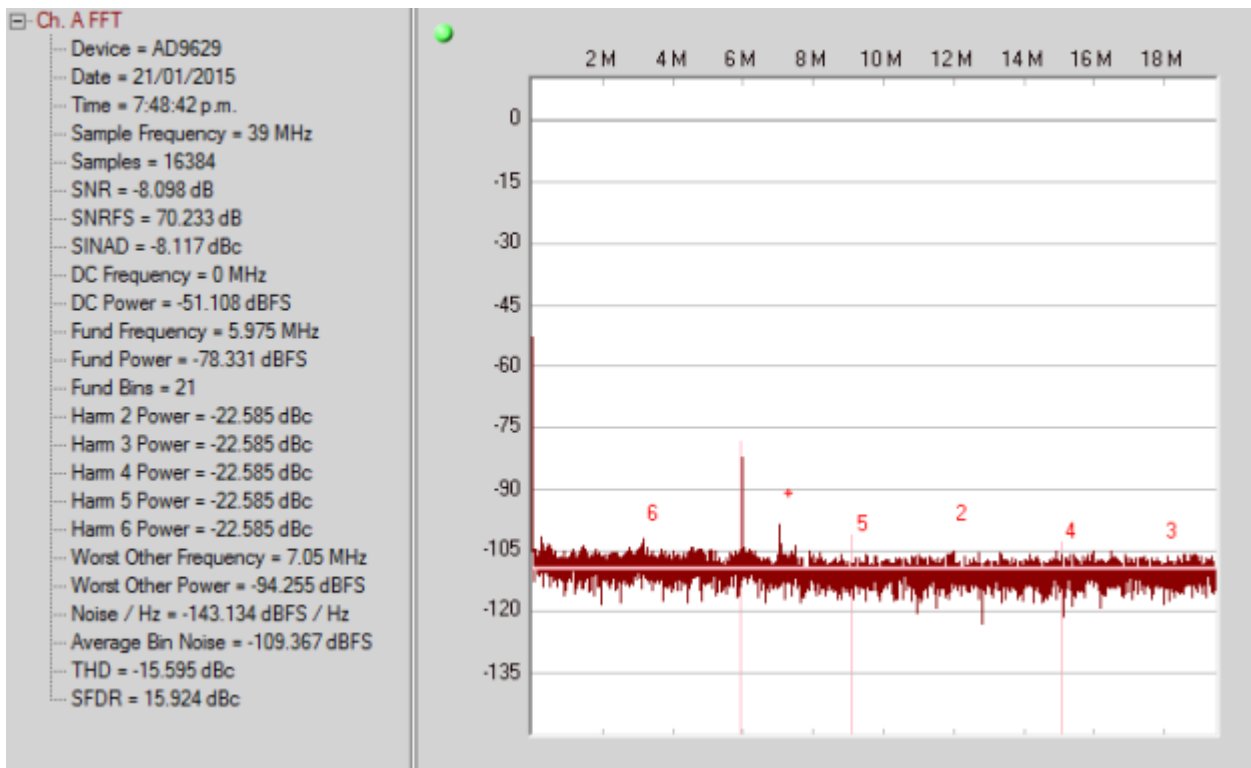


Figure 3.17: The FFT of the digitized signal with the input level lowered to -94dBm. This also illustrates a decrease in the ADC noise floor.

imposing the SFDR measurements was shown. Figure 3.16 demonstrates a new Worst Other Power at 5.375MHz, this harmonic has an amplitude of -51.442dBFS, which dominates the SFDR measurement. These harmonics remain at $\pm 600kHz$ from the carrier even as the carrier frequency is adjusted. The appearance of these harmonics look like they could be a product of some intermodulation, which typically occurs in a system when there are non-linearities [78]. It is very difficult to decipher where these harmonics have come from, as they did not appear in the analysis using the ADC evaluation board shown in Figure 3.7. The effect of these harmonics are not detrimental to the completion of the SDR platform. However, the issue of the unwanted harmonics at $\pm 600kHz$ from the carrier may corrupt other channels that reside in the Nyquist bandwidth, an investigation must be conducted in future work. For channel processing on the AIS signal shown in Figure 3.7, the harmonics can be filtered digitally from the Nyquist bandwidth. This is the beauty of SDR technology, once a signal has been successfully capture, further improvements to the SNR and dynamic range can be achieved using digital signal processing techniques.

3.5 SUMMARY

From this chapter, principle methods and techniques on implementing a AFE for direct digitalization was shown. The goal for the AFE is to utilize subsampling to capture the maritime bandwidth in the digital domain. Devising a frequency plan, which detailed the aliased component throughout the spectrum, provided an understanding of the sample rates and bandwidth required to image the maritime band into the Nyquist bandwidth. From the list of ADCs shown in Table 3.1, the available ADCs on the market from TI, ADI and Linear Technology were found. This presented the type performance and price range we could expect from the latest ADC devices. The AD9629, 40MHz ADC was chosen based on its price and performance. Figure 3.6 showed that using a sample rate of 39MHz could subsample the maritime bandwidth from the 9th Nyquist zone and centre it at 3.025MHz within the Nyquist bandwidth. The calculated process gain obtained by applying a sample rate of 39MHz is 29dB. This would reduce the channel noise floor achieving a SNR=98dBFS. An illustration of the improved noise floor was shown in Figure 3.4.

Using a high speed data capture kit, evaluation of the AD9629 was completed. Real-time data plots using FFTs with the aid of VisualAnalog verified that the AIS channel could indeed be successfully aliased from the 9th Nyquist zone. The digitized signal was then exported from VisualAnalog into MATLAB to simulated FM demodulation on the subsampled AIS signal. Comparisons of the demodulated signal using an HP8920A and MATLAB provided a sanity check for the demodulated waveform. This proof of concept verified that the subsampled AIS test signal was persevered throughout the direct digitization process.

Following the results gathered from VisualAnalog, designs for the AFE prototype were developed. Using the existing amplifiers and filters implemented on Vesper's Mimosa board, a signal chain was constructed as shown in Figure 3.14. Equation (3.5) calculated system noise factor, f_{sys} of the AFE signal chain using Friis's equation, the resulting system noise figure, NF_{sys} is 7dB. An AGC design was also added to the signal chain, for future developments on the prototype. The AFE obtained a total gain of 30dB using two LNAs.

The evaluation of the AFE prototype using the data capture board was shown in Figure 3.16. The measured full scale SNR is 47.261dBFS, falling well below the rated SNR of 69dBFS. The phase noise of the signal generator was a major contributor to the increase in noise. Decreasing

the input power on the signal generator to -94dBm increased the SNR to 70.233dBFS. Further work must also be done to investigate the unwanted harmonics that impede the SFDR measures. Optimizing the system at this stage will be included in the future work. The focus for the prototype is to implement direct digitization using subsampling. Tests on the AFE prototype showed a successful representation of the AIS signal in the digital domain, providing very encouraging results.

Chapter 4

DEVELOPMENT OF THE DIGITAL PLATFORM

In general, the term digital signal processing refers to the science of analysing a discrete-time signal, whose variables are quantized so that only the value of the signal at an instant of time is known [18]. The resolution and rate of these quantized variables are dictated by the ADC. From the prototype board completed in Chapter 3, the AD9629 produces a 12-bit discrete-time signal using a sample rate of 39MHz, that obtains an aliased version of an AIS channel. The goal of this chapter is to present the digital stages of the signal chain that completes the channel conversion to baseband. To execute digital signal processing on the subsampled maritime bandwidth, a discussion of the algorithms necessary to complete the signal chain is given. The digital signal processing will involve designing and developing a DDC. The implementation will be illustrated through the use of evaluation boards.

This chapter aims to select suitable programmable devices, and develop software that completes the SDR prototype. In Section 3.2.2, a proof of concept was presented, displaying FM demodulation on the subsampled AIS signal using MATLAB. This chapter will present real-time processing using programmable devices to achieve the AIS audio signal. With this milestone, an assessment of the SDR receiver platform can be done to relate the IEC receiver standards, verifying if the direct digitization receiver using subsampling is a feasible approach.

4.1 DESIGN OF THE DIGITAL SIGNAL CHAIN

The digital signal chain encompasses the remaining signal processing stages to down-convert the desired channel to baseband. At the output of the AD9629, AIS channel one lies at an aliased frequency centred at 5.975MHz (digital IF). In Section 1.3.2, an introduction to the digital front-end (DFE) signal chain was given, describing the process of converting the signal

from digital IF to its I and Q components. The quantized bandwidth goes through the DFE where channelization and sample rate conversion is executed, selecting, down-converting and down-sampling the channel of interest, an illustration is provided in Figure 1.5. This section will describe the development of the DFE signal chain used in the SDR platform. The algorithms required to obtain the baseband signal will be broken down to provide an idea of the digital hardware needed to execute the functions.

4.1.1 I and Q Demodulation

Executing demodulation at baseband typically requires the I and Q components of the signal of interest. I and Q data reveals the changes in amplitude and phase of a sine wave, providing information on the modulation. When these changes occur in an organized manner, information can be decoded from the sine wave [48]. Techniques to obtain the I and Q components vary in receiver structures.

As discussed in Section 2.5.1, the Q component corresponds to the quadrature phase shifted version of the I component. A common method to obtain a 90° phase shift in the digital domain is to use the Hilbert transform [79, 80]. However, the I and Q components must be acquired at baseband. Generally, modulation or demodulation on a channel is performed by using a NCO and multipliers to accomplish the frequency conversion [81]. The NCO is the digital version of the LO, used to create a discrete-time and discrete-valued representation of a sine wave. Equation (2.20) shows the general expression of a modulated carrier signal in its I and Q components. By generating two sine waves with a 90° phase shift difference at the NCO, the incoming signal can be separated into its I and Q components without the use of the Hilbert transform. This approach forms the concept of channelization, where the desired channel at digital IF is selected by tuning the NCO frequencies to convert the channel into its I and Q components at baseband. The generated signals from the NCO are fed into two separate multipliers for mixing operations to down-convert and produce the I and Q waveforms. A diagrammatic representation of the DDC structure is illustrated in Figure 4.1.

By generating a cos and -sin wave at 5.975MHz using the NCO, and multiplying it with the subsampled AIS signal on the respective I and Q channels, the I and Q data from AIS channel one will be acquired. This type of channelization structure is typically used in Direct Digital

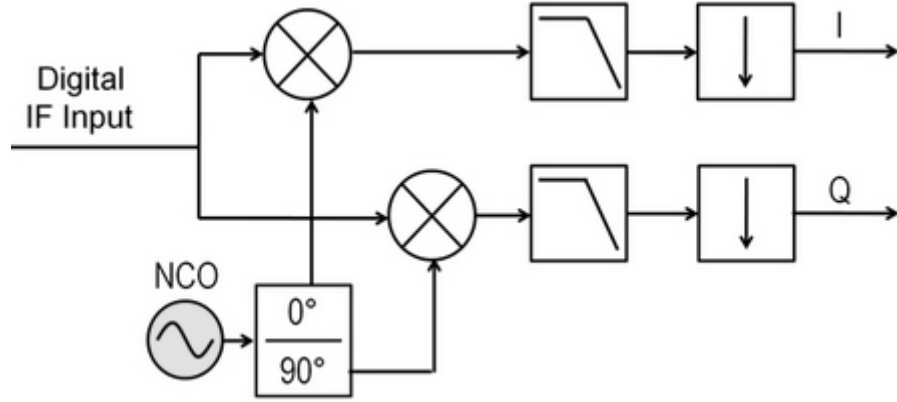


Figure 4.1: A typically DDC structure using a NCO to obtain the I and Q components [82].

Synthesizers (DDS), which are implemented in IC's. Devices such as the HSP50214B [83] show the use of the NCO for DDC functionality, these types of devices are generally used in digital receivers. There is a moderate level of programmability with the HSP50214B, however, they are physically restricted in the number channels. Moreover, the goal of this project is to design a platform that does not rely on single source components, and can be fully configured by software. As detailed in [16, 84], an FPGA can be used to implement wideband digital receivers with fully programmable features. The FPGA will allow the receiver design to incorporate multiple channels in the FPGA logic by configuring multiple DDC structures. Depending on the logic resources used to accomplish the DDC, the cost per device can be reasonably low, around the \$10 (USD) range. With this price in mind, FPGAs were investigated for the SDR platform. Discussion on the FPGA implementation continues in Section 4.2.

4.1.1.1 Quadrature Sampling Method

An alternative method that is also used to obtain the I and Q components is quadrature sampling with digital mixers [18]. This method is attractive because of its simplicity. The process of quadrature sampling requires the channel at digital IF, $f_{dig\ IF}$ to equal quarter the sample rate, f_s , that is, $f_{dig\ IF} = f_s/4$. If this condition is met then the generated cosine and sine waves used to separate I and Q components are:

$$\cos(2\pi f_{dig} IFn) = \cos(\pi f_s n/2) = \cos(\pi n/2) = 1, 0, -1, 0, \dots \quad (4.1)$$

$$-\sin(2\pi f_{dig} IFn) = -\sin(\pi f_s n/2) = -\sin(\pi n/2) = 0, -1, 0, 1, \dots \quad (4.2)$$

The repetitive four-elements, 1,0,-1,0, and 0,-1,0,1, will cycle at a rate of $f_s/4$. Therefore, the cos and -sin components will match the frequency of the incoming signal at $f_{dig} IF$. The structure of the quadrature sampling method is shown in Figure 4.2. Visually, the cos and -sin components can be pictured as two triangle waves represented by four samples per cycle with a frequency $f_s/4$, that have a 90° phase shift. Mixing these two triangle waves with the incoming signal converts the I and Q components to baseband. This method does not require a NCO, hence, it is possible to implement the I and Q demodulation in a DSP. The complexity of the quadrature sampling method shown Figure 4.2 suggests there is a small amount processing required.

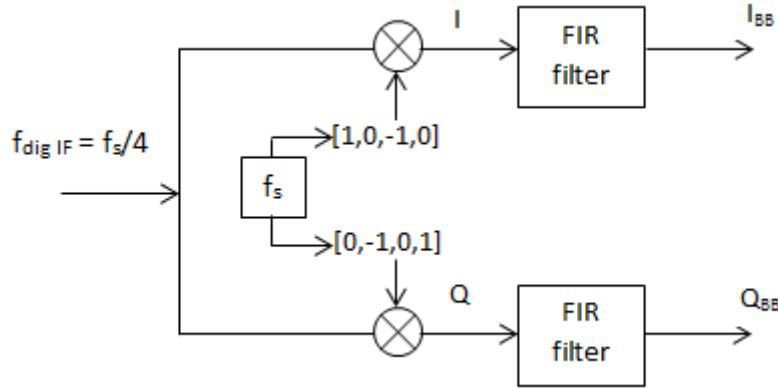


Figure 4.2: Illustration of the quadrature sampling method. The 1,0,-1,0, and 0,-1,0,1, sequences represent the cos and -sin waves receptively, obtaining a 90° phase shift to separate the I and Q components.

The pitfall in using the quadrature sampling method is that the receiver is only limited to one channel, which must be located at $f_s/4$. For this reason, quadrature sampling was only used for the analysis of the FM demodulation algorithm in the DSP. This analysis will be shown in Section 4.3.2.

4.1.2 Decimation using Cascaded Integrator-Comb Filters

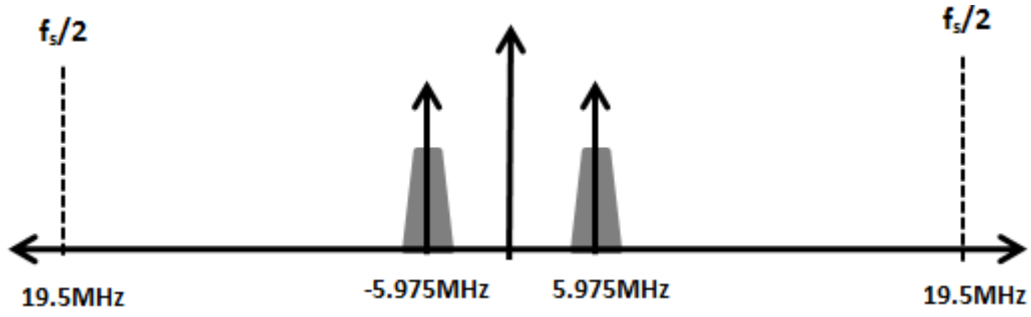
In acquiring the I and Q components of the desired channel at baseband, there is no longer any need for the entire 19.5MHz of digitized bandwidth ($f_s/2$). In Section 2.5.3, the process of

decimation described the method of down-sampling the digitized signal to discard the unused bandwidth. By reducing the sample rate by a factor of R , the Nyquist bandwidth is reduced to a bandwidth of $f_s/2R$. Figure 4.3 illustrates the process of channelization and decimation on the subsampled AIS signal at digital IF. Figure 4.3a shows AIS channel one aliased to 5.975MHz. Tuning a NCO to separate the channel into its I and Q components, as discussed in Section 4.1.1, results in the channel being converted to baseband. Figure 4.3b illustrates the bandwidth outside the channel at baseband. By decimating the 39MHz sample rate by a factor of $R=750$, results in a new sample rate, $f_{s\ new}=52\text{kHz}$. Figure 4.3c displays the spectrum after decimation, the Nyquist bandwidth now encompasses 26kHz, which is used to represent the AIS channel at baseband. The signal now captured in the new Nyquist bandwidth of 26kHz corresponds to the same signal in Figure 4.3b, that has been decimated by taking every 750th sample.

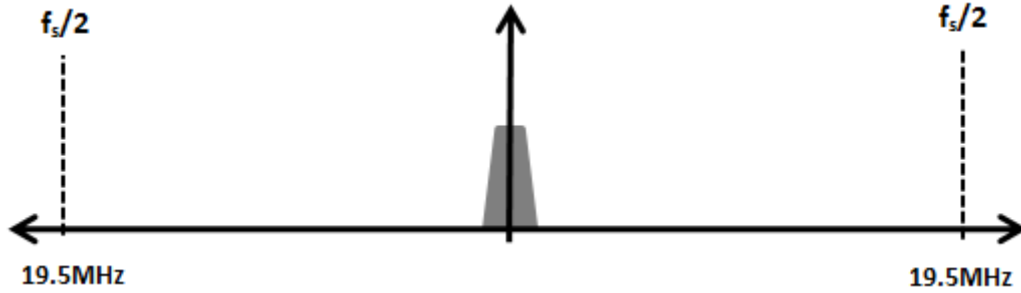
Figure 4.3c also demonstrates the aliased components in the neighbouring Nyquist zones. To provide the anti-aliasing filtering prior to decimation, high data rate filtering is typically applied before the decimation process. However, cascaded integrator-comb (CIC) filters are well suited for anti-aliasing filtering for decimation. Their frequency magnitude response envelopes are a similar slope to $\sin(x)/x$ [18]. Figure 4.4 shows the basic structure of the CIC decimation filter with N stages. At each the integrator stage a one-pole filter with a unity feedback coefficient is implemented [85]. The comb stages operates at f_s/R , each stage consists of a differential delay of M samples. The differential delay is a filter design parameter used to control the filter's frequency response [85]. The transfer function of an N^{th} order CIC filter is:

$$H(z) = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = \left[\sum_{k=0}^{RM-1} z^{-k} \right]^N \quad (4.3)$$

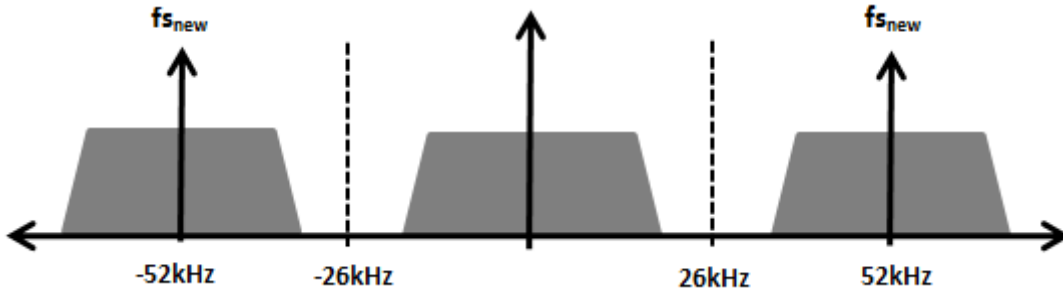
Using filter design and analysis (FDA) tools in MATLAB the magnitude response of the CIC filter can be simulated. Figure 4.5 shows the $\sin(x)/x$ response of the CIC filter. The CIC filter shown consists of $N=6$ stages, the comb section uses a differential delay of $M=2$, and the 39MHz sample rate is decimated to 52kHz by using a decimation factor of $R=750$. The differential delay of $M=2$ creates magnitude nulls at integer multiples of f_s/RM in the magnitude response of Figure 4.5. This not only acts as a low-pass filter for the baseband signals, but also creates null magnitudes to remove the neighbouring aliased components after decimation, as was shown in Figure 4.3c.



(a) The Nyquist bandwidth at the output of the ADC.



(b) The down-converted channel in its I and Q components at baseband. Illustrating the unused bandwidth.



(c) The decimated signal, resulting in a new sample rate, $f_{s\ new} = f_s/R$. The Nyquist bandwidth now encompasses 26kHz.

Figure 4.3: An illustration of spectrum after decimating the 39MHz sample rate by $R=750$. This results in a new sample, $f_{s\ new}$ of 52kHz.

The effect of averaging (or decimating) the 19.5MHz bandwidth to 26kHz also improves the SNR. In Section 3.1.2, the process gain achieved by filtering and decimating the 19.5MHz bandwidth to the channel bandwidth of 25kHz provided an extra 29dB to the full scale SNR. The only difference here is that the CIC filter has reduced the bandwidth to 26kHz to represent the channel. The increase of 1kHz to the channel bandwidth still provides approximately the same process gain. The real performance issue is the potential of aliased components in the 26kHz bandwidth that will increase the channel noise floor.

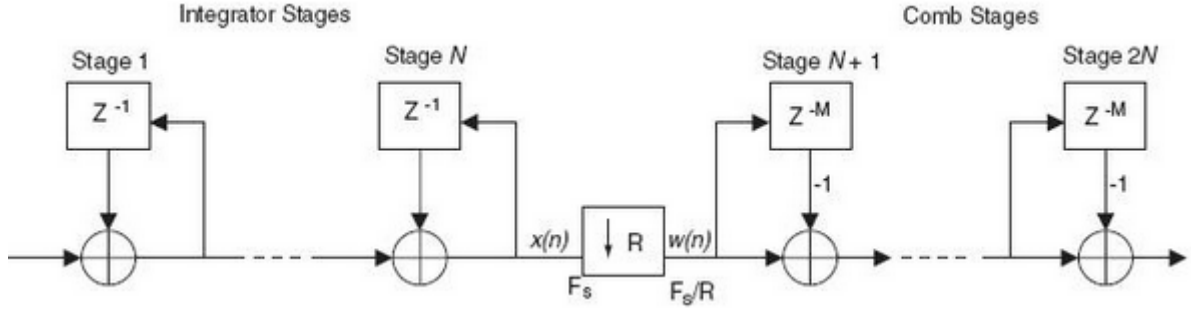


Figure 4.4: The CIC filter used for decimation, consisting of integrator stages followed by comb stages [86].

The benefits of reducing the sample rate to 52kHz means that the computational workload has also been reduced (in computations per second). Hence, the implementation of a DSP to encapsulate the AIS baseband processing is a viable option. Dedicating the FPGA to implement the DDC structure would mean the logic resource used would be focused on the I and Q demodulation and CIC filter implementation. The size of the FPGA would not need to be large to conduct the DDC functions, hence the cost per device would be relatively low. The next section discuss the hardware options to implement the DFE and baseband processing.

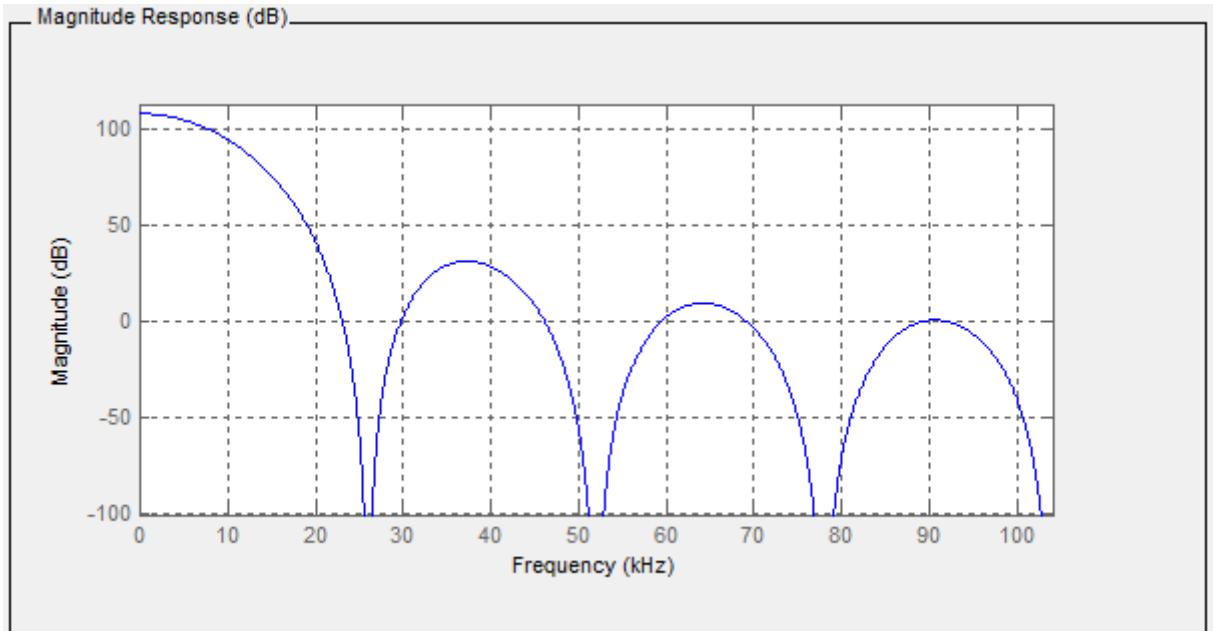


Figure 4.5: Magnitude response of the CIC decimation filter using FDA tools. Implementing a differential delay of $M=2$ and decimating by $R=750$. Null magnitudes lie at integer multiples of 26kHz.

4.2 DIGITAL HARDWARE REQUIREMENTS

The choice of digital hardware used for the SDR is completely dictated by the application. Moreover, the power and speed requirements to process the real-time bandwidth corresponds to the performance needed to carry out the DFE and baseband functions. This section focuses on the implementation of FPGAs and DSPs. The advancements in these technologies show promising features that provide the necessary processing for the SDR platform.

Implementing real-time processing at 39MHz can not be accomplished by commercial DSPs. Typically, any algorithms to be conducted on sample rates more than 10MHz will require a hardware configurable logic device like an FPGA. For example, if a DSP was used with a processor clock speed of 1GHz, and the signal to be processed is 39 MSps (mega samples per second) then only $1\text{G}/39\text{M}=25$ clock cycles are available to perform arithmetic on each sample. Processors can only perform one multiple and accumulate (MAC) per cycle. In an FPGA, thousands of MACs per clock cycle can easily be performed, making it very suitable for wideband applications [16, 87, 88]. For this particular reason, an FPGA will be chosen to carry out the channelization and sample rate conversion that forms the DDC. Section 4.1 showed the digitized AIS signal can be represented by a decimated sample rate of 52kHz. By partitioning the processing between a FPGA and DSP the processing load can be shifted so that the hardware effectiveness of the FPGA can be reduced and the processing load on the DSP is achievable.

It is possible to use an FPGA as a single chip solution. However, the cost of an FPGA to implement the DFE and the baseband processing algorithms of the CMX7032 will come at the cost of a bigger and more expensive device. Dedicating the FPGA to encapsulate the DDC functions only, allows more complex and heavy logic algorithms to be implemented in a DSP. Programming digital signal processing functions is more easily accomplished in DSPs, particularly when coding high level branching in the communication protocol stack [87]. Moreover, re-programmability is more easier when using a standard language like C.

4.2.1 The Digital Hardware Platform

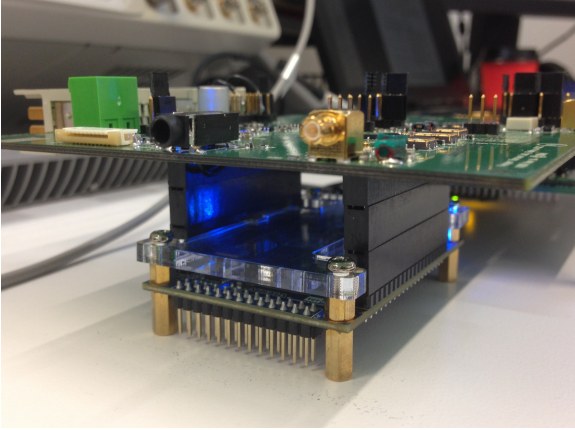
The FPGA and DSP devices are purchased in the form of evaluation boards so that hardware implementation is simple, and software can be developed in a “plug and play” fashion. There are a number of suitable FPGAs on the market such as Xilinx’s Spartan-6, Microsemi’s Igloo and

Lattice's MachX02, however, the Cyclone IV FPGA from Altera's low cost, low power family of FPGAs was chosen [89]. To evaluate the Cyclone IV family, the DE0-Nano evaluation Board was chosen, since its cost and simplicity of implementation made this board very suitable for the SDR prototype. The important specifications to consider from the DE0-Nano board are as follows [90]:

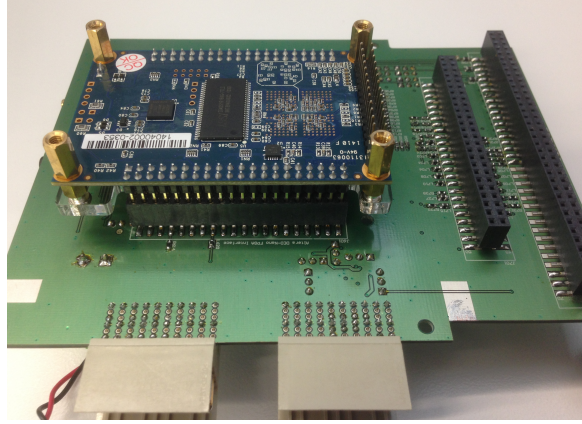
- Cyclone IV EP4CE22F17C6N FPGA.
 - 22,320 Logic elements (LEs).
 - 594 Embedded memory (kbits).
 - 66 Embedded 18 x 18 multipliers.
 - 153 Maximum FPGA I/O pins .
- Expansion Header.
 - Two 40-pin Headers (GPIOs) provides 72 3.3V I/O pins.
- Memory Device.
 - 32MB SDRAM.

The Cyclone IV, EP4CE22 is a relatively large FPGA costing \$44.40 per device (USD) [91]. However, the smaller devices in this family can cost as low as \$11.95 (USD) [92]. By using the larger FPGA we can safely evaluate the necessary DDC functions in the FPGA logic. It is expected that a fraction of the LEs and multipliers in the EP4CE22 will be used for the DDC functions. Coding the DE0-Nano board will identify the amount of resources needed, allowing us to specify the particular device in the family that fits the DDC implementation.

The 40-pin expansion header will provide access to 72 I/O pins, which is more than enough to feed in the 12-bit parallel port data from the AD9629, and feed out the down-converted data on a serial port. Figure 4.6 shows the connection between the analog front-end (AFE) prototype and the DE0-Nano board. The 12 data pins plus the clock pin on the AD9629 are streamed into the DE0-Nano board. The output data from the DDC will then get sent back to the AFE prototype board so it can be interfaced with the DSP.



(a) Side view of the DE0-Nano board connected to the AFE prototype board.



(b) Underneath the AFE prototype board the 40 pin connectors interface with the DE0-Nano board.

Figure 4.6: Physical interface between the AFE prototype board and the DE0-Nano board.

The DSP evaluation board chosen for the SDR platform is the BF526 EZ-LITE kit, from Analog Devices [93]. Other vendors such as TI were considered, however, the support and resources for the Blackfin DSP led to the decision to go with Analog Devices. The Blackfin, BF52X is a family of different DSPs with different features and memory sizes. The BF526 evaluation board provides the best Blackfin DSP of that family so that implementation can be analysed. The important parameters that were considered when selecting the BF526 are [93]:

- Processor core with up to 400MHz performance.
- On-chip memory of 132KB (use of L1 and L3 memory).
- 64MB synchronous dynamic random-access memory (SDRAM).
- Two dual-channel, full duplex serial ports (SPORT) supporting 8 I^2S channels
- Low standby power of 1mA and a sleep mode power of 50uA.

With a process speed of 400MHz, the BF526 has the capability to execute baseband algorithms with $400\text{MHz}/52\text{kHz}=7,692$ MACs per cycle, providing ample computational power to investigate and develop the baseband processing. The BF526 has 138KB of on-chip memory, there is also access to 64MB SDRAM should it be required. The SPORT interface will provide the SDR with the capability to process a maximum of eight channels. The BF526 costs \$10.76 (USD) per device [94]. However, DSP prices can be as low as \$1.99 (USD) per device [94]. The final

selection of the DSP cannot be made until full implementation is accomplished, this includes the encapsulation of FM demodulation and the CMX7032 AIS processing functions.

Figure 4.7 shows the hardware implementation of the AFE board and the BF526 evaluation board. The BF526 will conduct the FM demodulation to obtain the audio signal. Once this milestone is reached, the AIS audio signal can be analysed. Achieving the baseband signal for AIS processing will provide enough functionality to test the receivers signal-to-noise and interference (SINAD), this will be conducted in Chapter 5. The implementation of the AIS baseband processing functions in the DSP will not be investigated in this project. However, the SDR platform includes the capability to feed the FM demodulated signal into the CMX7032 chip to recover the VDM. The SDR platform developed will have the capability to investigate CMX's functions in the baseband subsystem for future developments.

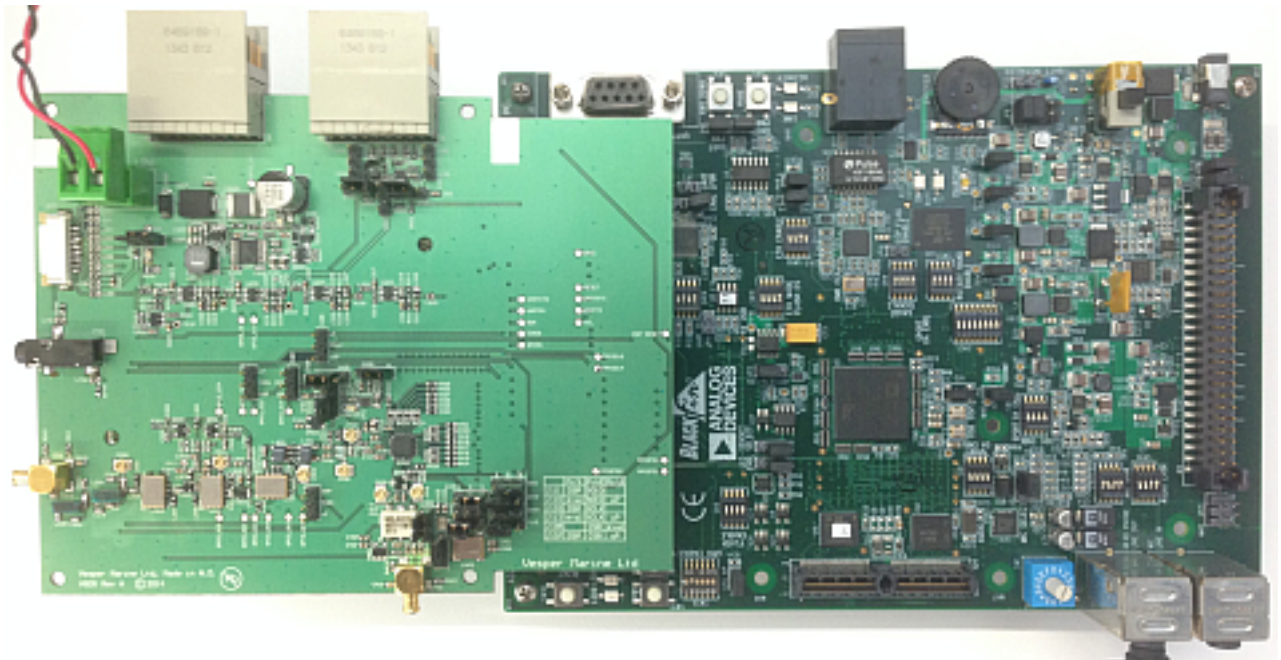


Figure 4.7: The structure of the AFE prototype board and the BF526 evaluation board. Note the DE0-Nano board it connected underneath the AFE board.

4.2.2 Data Interfacing throughout the Signal Chain

The digital signal chain processing stages in the SDR platform can be described by the diagram presented in Figure 4.8. The maritime bandwidth at digital IF is streamed into the DE0-Nano Board at 39MHz. The 12-bit parallel data from the AD9629, including the 39MHz clock, is

interfaced with the I/O pins on the DE0-Nano board's expansion header. Within the FPGA the DDC structure, as detailed in Section 4.1.1 and Section 4.1.2, is formed to produce the I and Q components at a decimated rate of 52kHz.

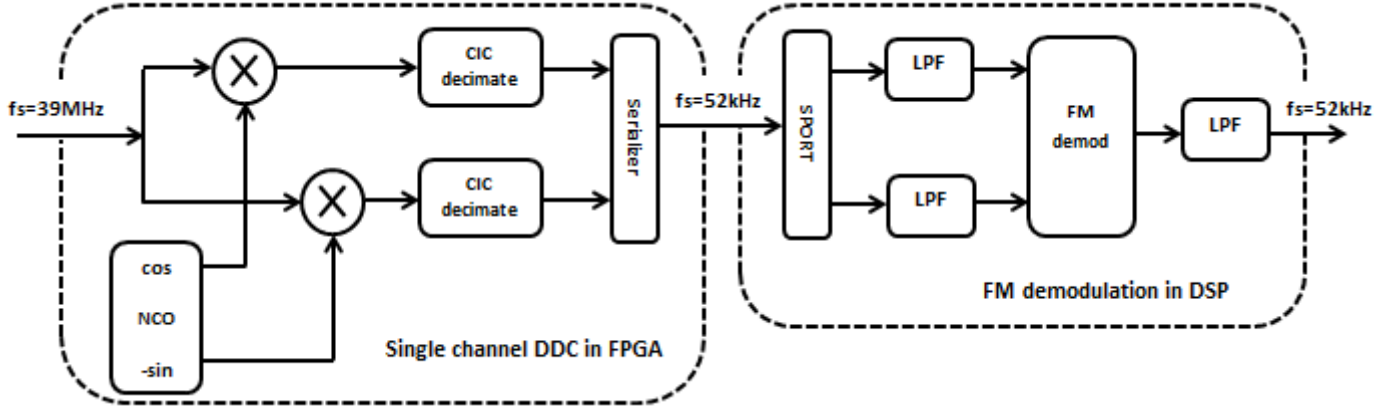


Figure 4.8: An overview of the digital signal chain from digital IF to the demodulated message signal.

The I and Q data enters the DSP on a 32-bit data bus, streaming at 52kHz. A minimum of three pins can be used to stream the data via the SPORT interface. These are the clock (CLK), data and the frame sync (FS) pins. Using a frame size of 32-bits, the I and Q data can be interfaced on a single pin, having 16-bit I data and 16-bit Q data, as illustrated in Figure 4.9. By using the FS pin we can easily separate the I and Q data in the DSP. The I and Q components are fed through a LPF respectively, the FM demodulation algorithm then uses the I and Q data to obtain the message signal.



Figure 4.9: An illustration of the 32-bit frame containing the 16-bit I data and 16-bit Q data.

An audio codec (SSM2603) is also included on the BF526 evaluation board, which has two DACs [95] . By outputting the demodulated signal from the DSP into the codec's DACs, the analog representation of the AIS audio signal can be observed through a scope. Moreover, the AIS data processing can also be conducted by feeding the AIS audio signal into the CMX7032.

4.3 SOFTWARE DEVELOPMENT

Development of the software was done in two parts. Implementation of the DDC within the DE0-Nano board was accomplished by Brindsley Archer. In parallel, the implementation of the FM demodulation with the BF526 evaluation board was achieved by myself. This section will detail the development process of the FM demodulation software, and touch on the hardware logic executed in the FPGA by Brindsley.

4.3.1 The Digital Down Converter

Credit must be given to Brindsley Archer for his work on the project. He worked on the DDC implementation with the DE0-Nano board and accomplish an efficient method to output the decimated I and Q waveforms. Brindsley also incorporated the capability to receive two channels simultaneously by using two DDC structures in the FPGA. The amount of FPGA resources used on the Cyclone IV, EP4CE22 for the two channel DDC structure is shown in Figure 4.10. The amount of logic elements, memory and multipliers used are only a small fraction of the full capacity on the EP4CE22. Therefore, a much smaller FPGA can be used to implemented the DDC. Table 4.1 shows the Cyclone IV family of FPGAs [89], the EP4CE6 is the smallest FPGA in the family and costs \$11.95 (USD) [92]. The DDC implementation will only use a small portion of the FPGA hardware in this device. However, the limiting factor is the use of two phase-locked loops (PLL) needed for the NCO in each channel.

Total logic elements	1,917 / 22,320 (9 %)
Total combinational functions	1,343 / 22,320 (6 %)
Dedicated logic registers	1,690 / 22,320 (8 %)
Total registers	1690
Total pins	25 / 154 (16 %)
Total virtual pins	0
Total memory bits	9,600 / 608,256 (2 %)
Embedded Multiplier 9-bit elements	12 / 132 (9 %)
Total PLLs	2 / 4 (50 %)

Figure 4.10: The amount of FPGA resources used on the Cyclone IV, EP4CE22 to implement two DDC structures for two channels.

Development of the DDC using the DE0-Nano board has provided the information needed to optimize the SDR prototype. From the implementation a good estimate of the necessary resources for more channels can be formed. This project only goes as far as implementing two channels in the SDR prototype.

Resources	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Logic elements (LEs)	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
Embedded memory (Kbits)	270	414	504	594	594	1,134	2,340	2,745	3,888
Embedded 18×18 multipliers	15	23	56	66	66	116	154	200	266
General-purpose PLLs	2	2	4	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20	20
User I/O Banks	8	8	8	8	8	8	8	8	8
Maximum user I/O ⁽¹⁾	179	179	343	153	532	532	374	426	528

Table 4.1: Table of the Cyclone IV FPGA family, displaying the FPGA resources in each device [89].

4.3.2 FM Demodulation

In Section 2.6.1, an expression was formulated to obtain the instantaneous frequency using the I and Q components. Equation (2.34) provides an expression to obtain the FM message signal without the use of the arctangent operator. To evaluate Equation (2.34) using the DSP, the I and Q components must be acquired. Since the FPGA software was developed in parallel with the DSP software, the DSP temporarily incorporated the I and Q demodulation stage using the quadrature sampling method. In Section 4.1.1, it was shown that the NCO was not required to perform I and Q demodulation when implementing the quadrature sampling method. However, the condition of $f_{dig\ IF} = f_s/4$ must be met. In order to stream the subsampled data, an interface board was created to connect the ADC evaluation board to the BF526 evaluation board. The interface board routes the data and clock pins into the expansion header on the BF526 evaluation board, so the subsampled data can be processed. Figure 4.11 shows the interim platform used to develop the FM demodulation software.

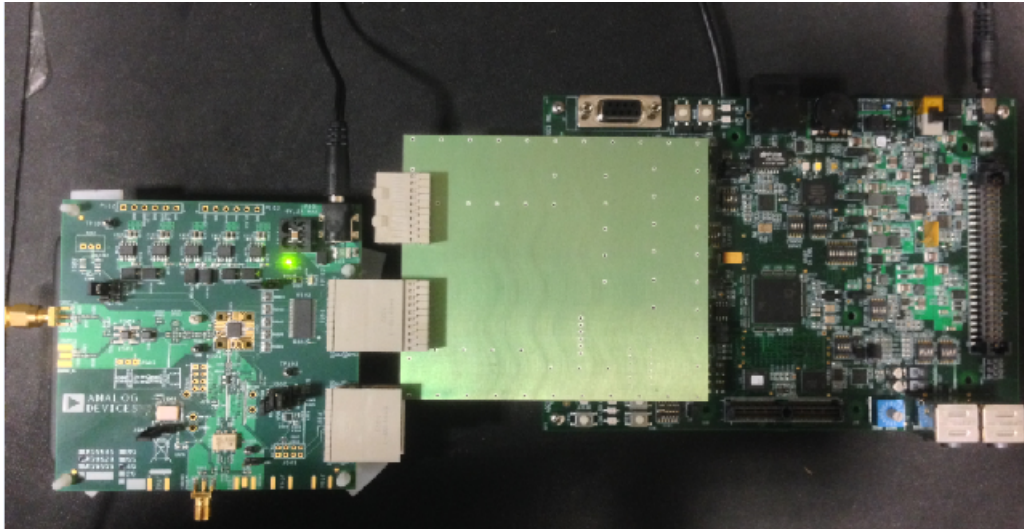


Figure 4.11: The hardware platform used to develop the FM demodulation algorithm.

The sample rate of 39MHz had to be re-evaluated so that the DSP has ample MACs to execute the algorithms. The chosen sample rate to drive the AD9629 is 1MHz, providing $400\text{M}/1\text{M}=400$ clock cycles per sample. Obviously, the RF signal at 161.975MHz could not be used for the interim platform, so an FM modulated signal was generated on a carrier of 4.25MHz. With this frequency plan, the 4.25MHz carrier will be subsampled to a digital IF at 250kHz. Therefore, the $f_{\text{dig IF}} = f_s/4$ condition is met to execute the quadrature sampling method.

Figure 4.12 illustrates the processing stages in the DSP to conduct the FM demodulation algorithm. The 12-bit data enters the BF526 via it's PPI. Direct memory access (DMA) capabilities allow the DSP to store the 12-bit data in memory without dependence on the processor. It is important that the DSP stores and processes the incoming data in real-time. To aid real-time processing, a ping-pong buffer configuration was used within the DMA. This method consist of two circular buffers called "ping" and "pong" that alternate between being filled with data and being processed. For example, as the "ping" buffer is being filled by the DMA, the "pong" buffer gets processed simultaneously. The buffers are interrupt driven, so that when one buffer has been filled by the DMA an interrupt service routine (ISR) is triggered, alternating the buffers for processing.

Once the buffer is sent to the processor, I and Q demodulation is implemented using the quadrature sampling method. Appendix A shows the `Process_Data()` function used in software to execute each of the digital signal processing stages in Figure 4.12. After low-pass filtering

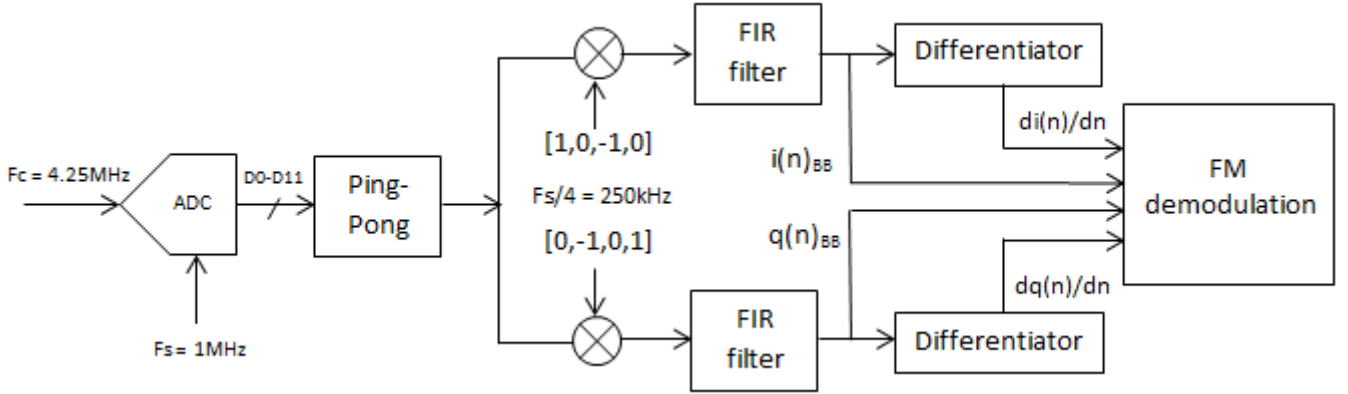


Figure 4.12: Diagram of the processing stages executed in the DSP to perform FM demodulation.

through FIR filters, the I and Q components are fed into a differentiator to obtain the $i'(n)$ and $q'(n)$ values. By programming the expression in Equation (2.34) into the DSP the message signal can be recovered.

Using a signal generator, a 4kHz squarewave was modulated onto the 4.25MHz carrier. The structure shown in Figure 4.12 was programmed into the BF526 to observe the squarewave at the output of the FM demodulator. This step provides a simulation of the FM demodulation stage when obtaining the AIS audio signal.

The software environment used to code the BF526 is Analog Device's CrossCore Embedded Studio (CCES). This environment provides a lot of flexibility to debug and observe data. Figure 4.13 displays the plot window in CCES of the output buffer with a size of 1024 samples. The FM demodulated signal shows that the wavelength of the squarewave consists of 250 samples per cycle. Therefore, the frequency is $1\text{MSps}/250=4000$, representing the modulated 4kHz squarewave.

At the completion of the FM demodulation process, the AFE prototype, DE0-Nano board and BF526 evaluation board were interfaced to form the complete receiver signal chain. The

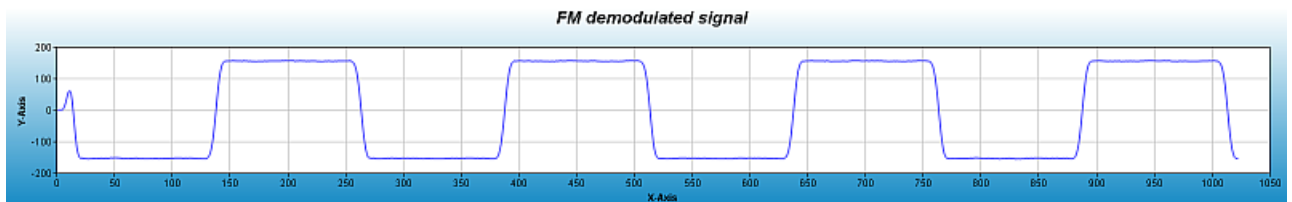


Figure 4.13: The FM demodulated waveform plot in CCES.

software used in the BF526 was altered to receive the serial I and Q data from the FPGA. This alteration is done by using the SPORT interface instead of the PPI on the BF526 and removing the quadrature sampling method from the code. The remaining LPFs, differentiators and the FM demodulator are then left to be executed in the DSP software. In the future, the DSP code can be developed further to incorporate the AIS baseband processing that complete AIS receiver functions.

4.4 SUMMARY

This chapter presented the design and development of the DFE and FM demodulation. In Section 4.1, the design of the digital signal chain proceeding the AD9629 was detailed. Channelization through the use of a NCO to implement I and Q demodulation was described. By obtaining the I and Q components at baseband, the Nyquist bandwidth can then be reduced through the process of decimation. The DDC structure used for the SDR incorporates a CIC filter, providing anti-aliasing capabilities so that the aliased components do not corrupt the baseband signal. The 39MHz sample rate was decimated by a factor of 750 to lower the sample rate down to 52kHz, and reduce the computational workload. It also improves the SNR through process gain.

In Section 4.2, the hardware requirements to implement the digital signal chain were discussed. The SDR platform consists of a FPGA followed by a DSP. The principle idea is to implement the wideband processing in the FPGA, which executed the DDC functions to obtain the I and Q components at a sample rate of 52kHz. At this speed, a DSP can be used to implement the baseband processing. This platform will allow the implementation of the CMX functions to be done by the DSP. By dedicating the FPGA as a DDC, only a fraction of the FPGA resources were required. It was concluded that the EP4CE6 provided a more optimal size for the SDR platform, costing \$11.95 [92].

Using the platform shown in Figure 4.11, the FM demodulation expression in Equation (2.34) was implemented in the BF526. The quadrature sampling method was used to obtain the I and Q data. The interim platform achieved a successful demodulated signal within the DSP, this step provides the AIS audio signal required to implement AIS data processing. From the developments of the DFE and FM demodulation in this chapter the SDR platform can be formed to implement the full receiver signal chain.

Chapter 5

SDR PROTOTYPE RESULTS

This chapter analyses the SDR platform as a whole by conducting test methods that relate to the IEC standards. The test methodology will focus on investigating the receiver's sensitivity and also its performance with multiple channels. The required receiver test parameters from the IEC 62287-1 standard shown in Table 2.1 will be referred to, providing a comparison to the required performance for AIS applications. The approach is to apply the designs developed in Chapter 3 and Chapter 4 that complete the receiver signal chain that recovers the AIS audio signal from the AIS channel. To quantify the performance of the output audio signal, SINAD measurements using the HP8920A will be performed. The evaluation of the SDR will also include the extension of the AIS data processing by interfacing the CMX7032 chip. This will provide final stage in completing the entire receiver process for AIS applications by obtaining the VDM data from the AIS signal.

The test results gathered from this chapter will ultimately identify the feasibility of the SDR receiver platform. Performance and cost comparisons will be made, where possible, between the SDR and the Mimosa board. Further discussion on improvements to the system will also be raised so that the SDR prototype can progress towards a commercial product.

5.1 SDR TEST STRUCTURE

The analog front-end (AFE) prototype is designed as the interface for the evaluation boards and the Mimosa board. Figure 5.1 demonstrates the signal paths throughout the SDR platform that connects all boards to complete the signal chain. The SDR test structure has the capability to feed two input channels. Signal generator one is the Marconi 2955B communications test set [96] and signal generator two is the HP8920A. As described in Section 3.3, the AFE prototype

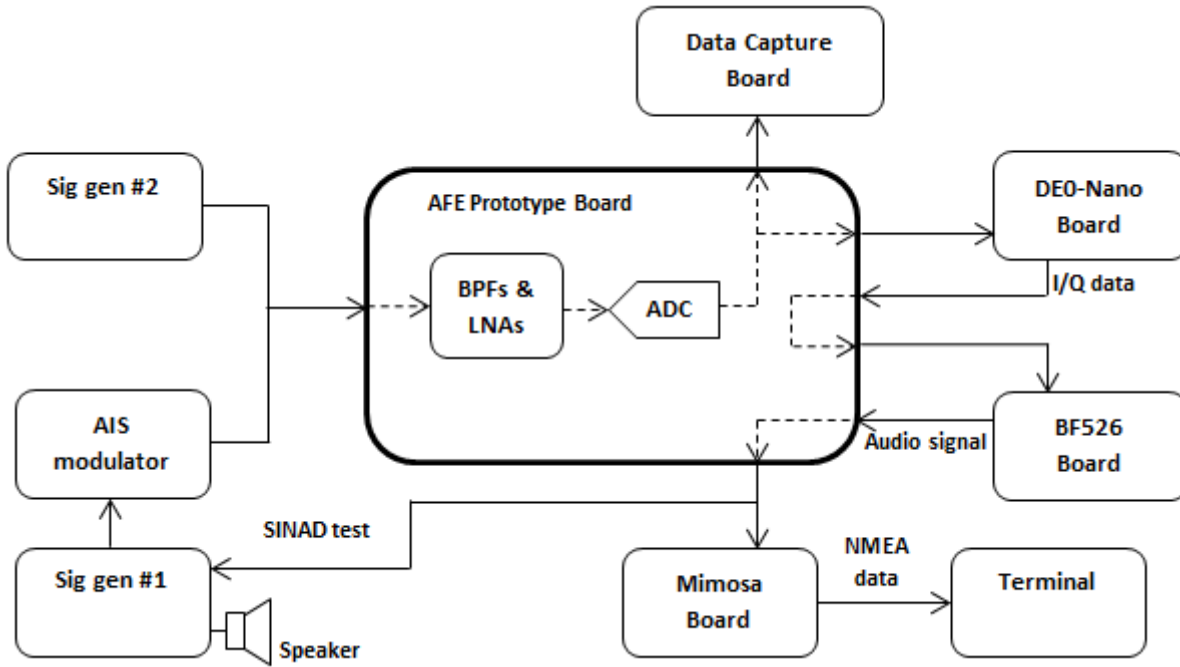


Figure 5.1: Diagram of the complete SDR, illustrating the signal path throughout the SDR platform.

board utilizes a direct digitization architecture, which will subsample the incoming signals from the signal generators. After the AD9629 completes the analog-to-digital conversion, the 12-bit data can be analysed by the data capture board, providing real-time feedback on the quantized bandwidth. To complete the conversion to baseband, the 12-bit data can also be sent into the DE0-Nano board. The DDC functions discussed in Section 4.1 are performed by the DE0-Nano board, producing the I and Q data. The I and Q data is then fed back to the AFE board, and sent to the BF526 evaluation board to conduct the discrete FM demodulation algorithm expressed in Equation (2.34). The BF526 evaluation board uses an audio codec to do a digital-to-analog conversion on the AIS audio signal. The CMX7032 chip on the Mimosa board uses the AIS audio signal from the codec to complete AIS data processing. By obtaining the VDM data at the output of the CMX chip, a terminal emulator known as Tera Term is used via a PC to display the VDM sentences.

The NMEA formatted data, provides packets of VDM/VDO sentences. VDM messages are AIS reports from other vessels, and VHF data-link own vessel (VDO) messages carry your own ship's data. These packets contains information such as position and course used for collision

avoidance applications. To observe each received VDM packet from the SDR test structure, Tera Term provides a graphical interface on a PC. Using signal generator number 1 with the AIS modulator, a AIS test message can be modulated onto a carrier and fed into the SDR. Running the test structure shown in Figure 5.1, the VDM sentence can be obtained using Tera Term. A typical VDM data packet is display as follows:

```
!AIVDM,1,1,,B,177KQJ5000G?tO`K>RA1wUbN0TKH,0*5C
```

This is an ASCII format for VDM representations of AIS messages. Decoders are used to retrieve the AIS information. An example of the information decoded from the VDM packet above is shown in Figure 5.2. This AIS information is used to identify and plot surrounding vessels on a graphical display, as was illustrated in Figure 2.1.

```
!AIVDM,1,1,,B,177KQJ5000G?tO`K>RA1wUbN0TKH,0*5C
```

```

Message sent (UTC) : 03:54:15
MMSI               : 477553000
Latitude           : 47.582833°
Longitude          : -122.345832°
Speed              : 0.0 knots
Heading            : 181°
Course over ground : 51°
Rate of turn       : 0°/min
Navigational status: 5
Nearest place      : Seattle, United States

```



Figure 5.2: AIS information decoded from the VDM packet. The location of the AIS unit transmitting is in Seattle [97].

Tests conducted using the SDR will not measure the PER of the received VDM packets. However, observing the VDM packet using Tera Term will show that the SDR platform has successfully implemented the receiver functions to recover the AIS information. In Figure 5.1, the audio signal can also be tested for SINAD to determine the receiver's sensitivity performance. Discussion on measuring the signal quality in the SDR is continued in the following section.

5.1.1 Signal Quality Throughout the SDR Platform

In Section 3.4.2, the signal quality of the subsample AIS channel was observed. It was found that AIS channel one (161.975MHz) was successfully aliased by the AD9629 to 5.975MHz. Figure 4.8 shows the digital signal processing stages that follows the analog-to-digital conversion. The first process in the digital signal chain is the DDC, which selects the subsampled AIS channel at 5.975MHz, and converts it into I and Q data. To observe the I and Q components fed from the FPGA into the DSP, the FFT plot window in CCES is used. Figure 5.3 displays a FFT of the I component fed into the BF526. Note that BF526 implements LPFs on the I and Q components respectively, with a cut-off frequency at 8kHz. From Figure 5.3 we can see that the I component has been successfully captured in the DSP with a signal level of approximately -91dBm. The input signal used for the test shown in Figure 5.3 is generated by signal generator number 1, with the AIS modulator, the signal level fed into the AFE board is -97dBm on AIS channel one (161.975MHz).

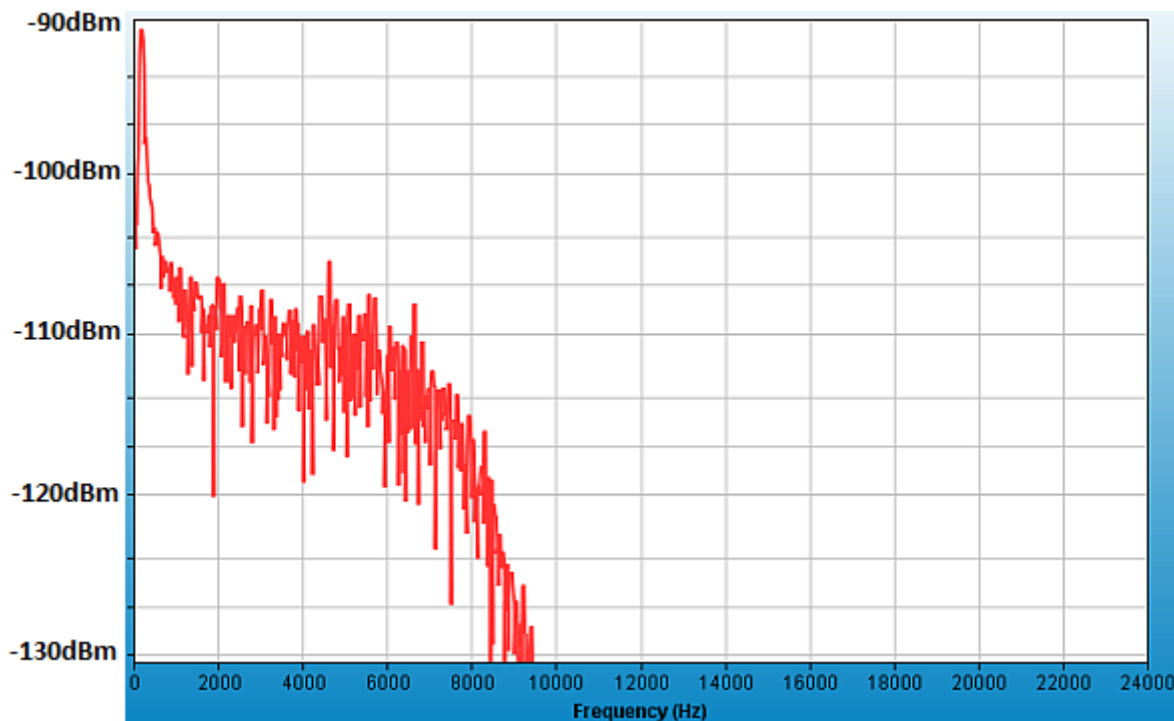
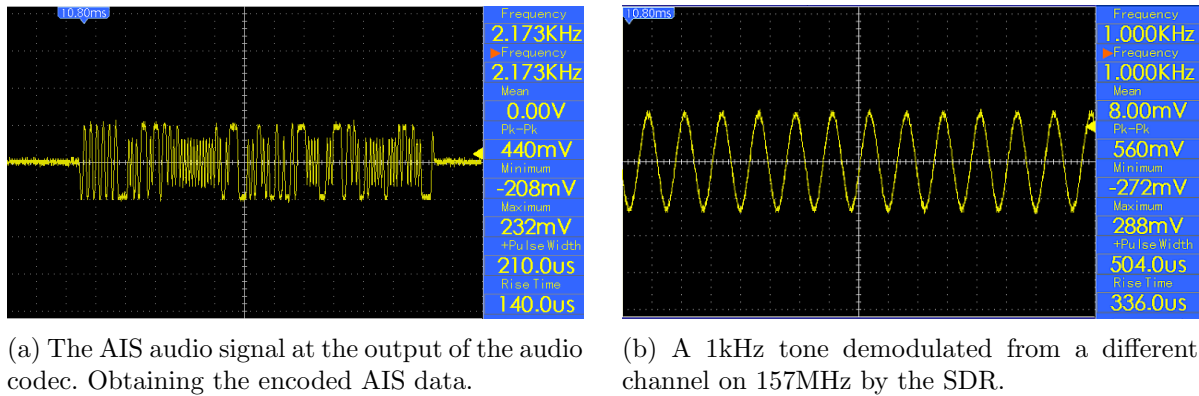


Figure 5.3: FFT of the in-phase component captured in the DSP. Note, a LPF has been implemented, with a cut-off frequency at 8kHz.

Obtaining the I and Q components allows the use of the FM demodulation expression shown

in Equation (2.34) to be implemented in the DSP. In Section 4.3.2, FM demodulation was accomplished using the interim platform, shown in Figure 4.11. Note that the FM demodulation used in the SDR is implemented without the quadrature sampling method. The resulting audio signal is then sent to the audio codec to be converted to the analog domain. The audio signal at the output of the audio codec is shown in Figure 5.4a, the encoded 1's and 0's within the message signal provides the data for AIS baseband processing. The CMX7032 uses the audio signal to produce the NMEA formatted data.



(a) The AIS audio signal at the output of the audio codec. Obtaining the encoded AIS data.

(b) A 1kHz tone demodulated from a different channel on 157MHz by the SDR.

Figure 5.4: An illustration of two demodulated waveforms on separate channels being received simultaneously.

The FM demodulation process can also be tested by the sound quality of a tone. By modulating a tone on the carrier instead of an AIS signal we can also produce a tone via speaker on the RF communications test set. Figure 5.4b shows a 1kHz tone demodulated from a different channel at 157MHz. The 1kHz tone can be heard via speaker. This test is conducted simultaneously with the AIS channel demodulation shown in Figure 5.4a, demonstrating a dual channel receiver.

Receiver performance can also be done by doing SINAD tests on the Marconi 2955B test set. SINAD is expressed in dB and is commonly quoted alongside the receivers sensitivity, providing a quantitative evaluation of performance [98]. As the received RF signal gets weaker it becomes progressively lost in the noise and distortion generated in the receiver. By convention, the accepted SINAD measure for intelligible speech on narrow band FM voice radio is 12dB [99]. The evaluation of the SDR platform will be based of the SINAD levels achieved from each the test condition applied. The SINAD test methods and results will be discussed in Section 5.2.

The final step in the receiver signal chain is the AIS baseband processing by the CMX7032 chip. Interfacing the AIS audio signal from the BF526 evaluation board to the CMX's input

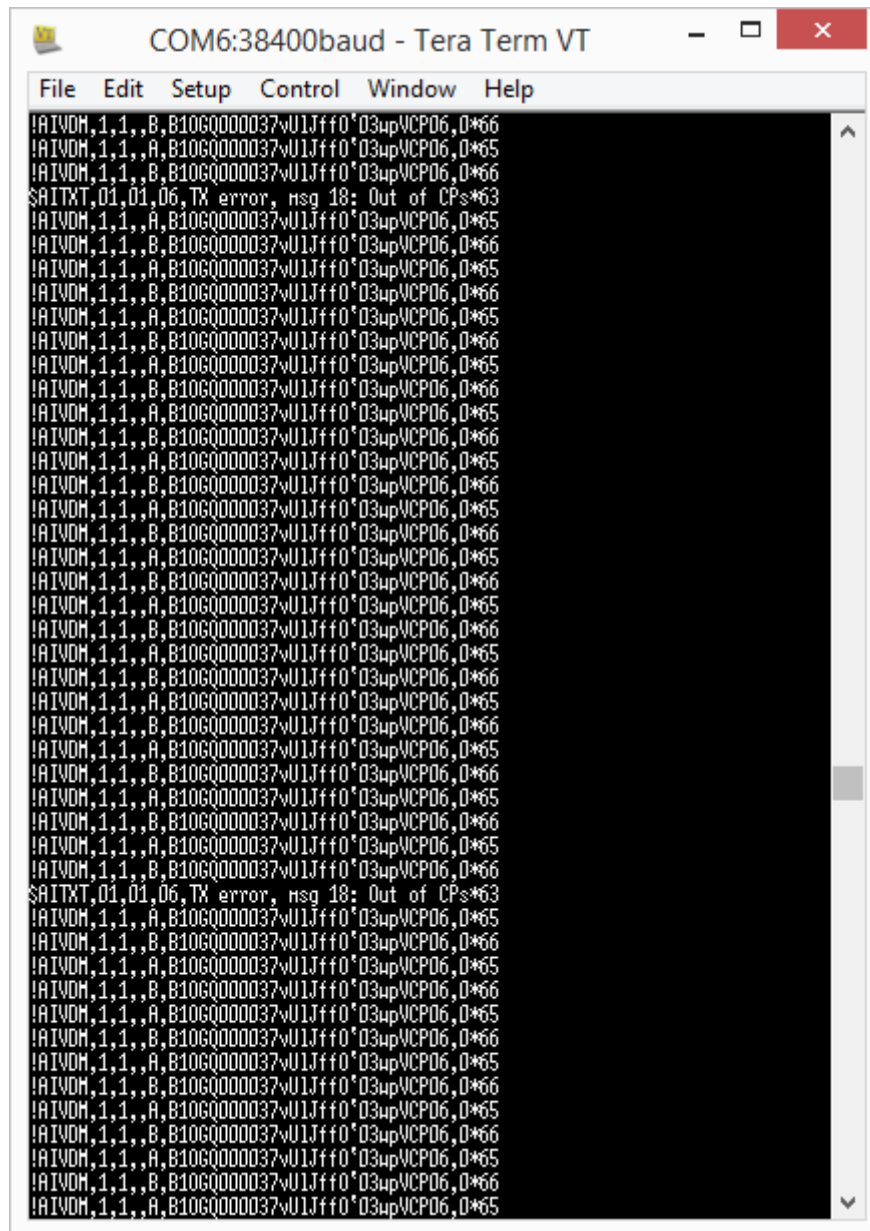


Figure 5.5: The VDM sentences displayed using the Tera Term software.

ports on the Mimosa, the NMEA data is obtained and sent to a terminal via PC, as illustrated in Figure 5.1. A baud rate of 38400bps is streamed to the terminal. Figure 5.5 displays the VDM sentences using the Tera Term software. Each VDM sentence is the same for each tests and are repetitive whilst the signal generator is transmitting. Figure 5.5 shows two cases where the packet is lost, denoted by the Tx error message. This test method used is only applied to proves that the SDR test platform is capable of producing VDM sentences. PER tests will be performed in future work.

Out of interest, speech over FM voice radio was accomplished using a VHF antenna at the input connector of the SDR platform. A portable radio was used to transmits speech over the 157MHz channel. Using a speaker, the speech was recovered. Simultaneously, an AIS channel one was also fed into the SDR input connector so voice on 157MHz and AIS information on 161.975MHz can be received. This showed that the SDR could implement an extra channels by simply adding it into the software, similar to the test shown in Figure 5.4.

5.2 TEST METHODS AND RESULTS

The objective of the tests conducted in this section aim to verify if the direct digitization architecture designed for the SDR can achieve performance that meets the receiver parameters for AIS, shown in Table 2.1. The tests accomplished in this section do not use PER to quantify the receiver performance. Tera Term provides a visual for the VDM packets received, but does not calculate the PER. Instead, SINAD tests are used to evaluate the audio signal produced by the FM demodulator. It is assumed that if a SINAD of 12dB is achieved then the PER will generally be greater then 20%. The tests conducted are as follows:

- Sensitivity
 - Maintain a SINAD of 12dB at the receiver's sensitivity.
- Error at high input levels.
 - Obtain the audio signal at a high input level of -7dBm.
- Co-channel rejection
 - The wanted signal at -101dBm must maintain a SINAD of ≥ 12 dB in the presences of an unwanted signal at -111dBm on the same channel.
- Adjacent channel sensitivity
 - The wanted signal at -101dBm must maintain a SINAD of ≥ 12 dB in the presences of an unwanted signal at -31dBm, ± 25 kHz from the wanted signal.
- Blocking
 - The wanted signal at -101dBm must maintain a SINAD of ≥ 12 dB in the presences of an unwanted signal at -15dBm, ± 5 MHz from the wanted signal.

Each test will use AIS channel one (161.975MHz) as the wanted signal. This will be generated by signal generator number 1, with the use of the AIS modulator. Signal generator number 2 will be used as the unwanted signal. The two signals are combined using a coupler, which feeds the signals into the SDR input, as shown in Figure 5.1. The hardware configuration of the SDR platform is displayed in Figure 5.6. The SINAD tests will determine the receiver performance, whilst Tera Term provides a visual of the packets being successfully received.

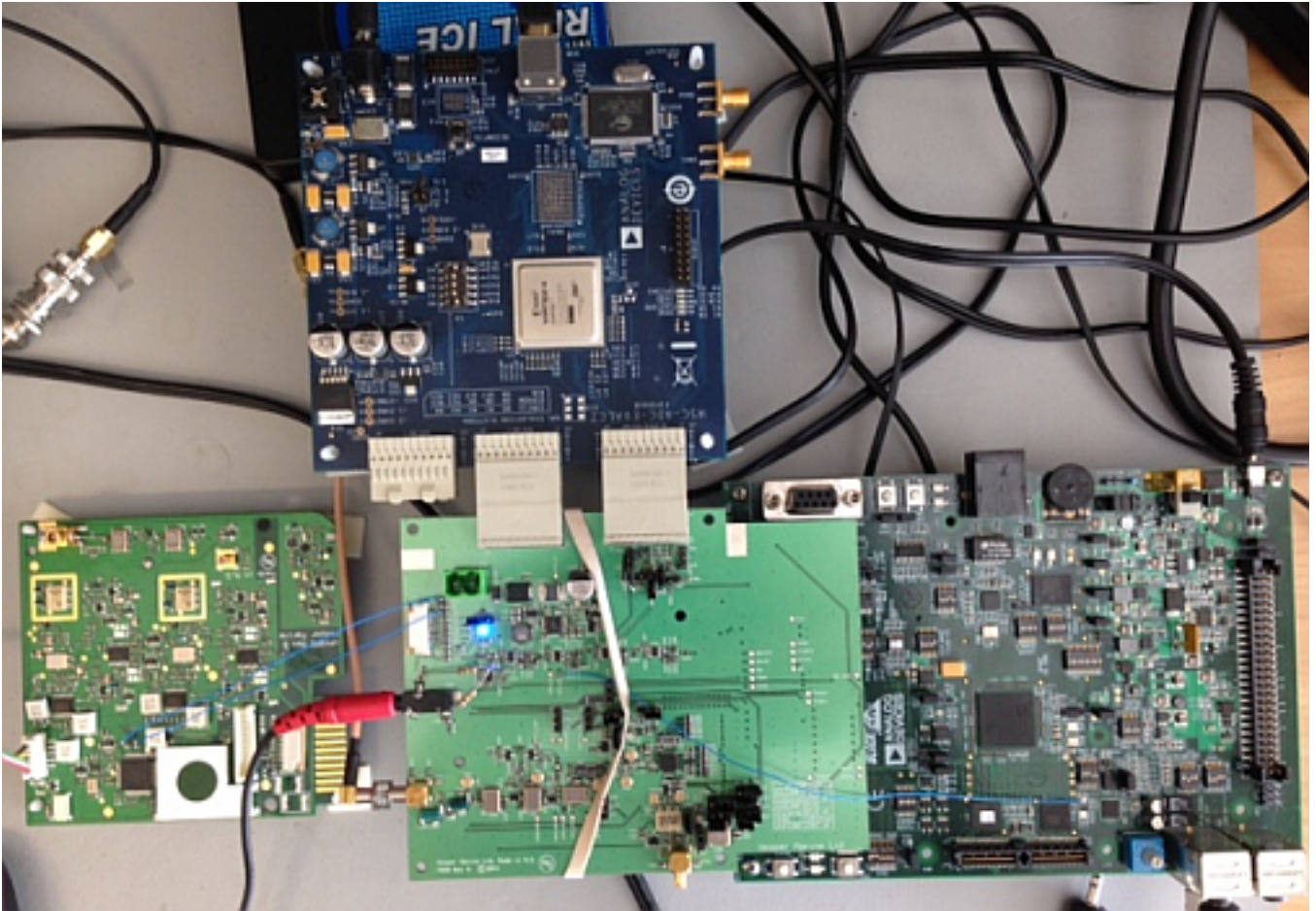


Figure 5.6: The complete hardware configuration of the SDR. Displaying the set up of the AFE board (middle), data capture board (top), DE0-Nano board (underneath AFE board), BF526 evaluation board (right) and the Mimosa board (left).

The sensitivity test was performed by adjusting the input signal level until the SINAD on the Marconi 2955B test set reaches 12dB. The input signal used was FM modulated using a 1kHz sine wave with a deviation of 3kHz. The demodulated signal was sent from the output of the audio codec to the 2955B test set to perform SINAD measurements. Figure 5.7 shows the

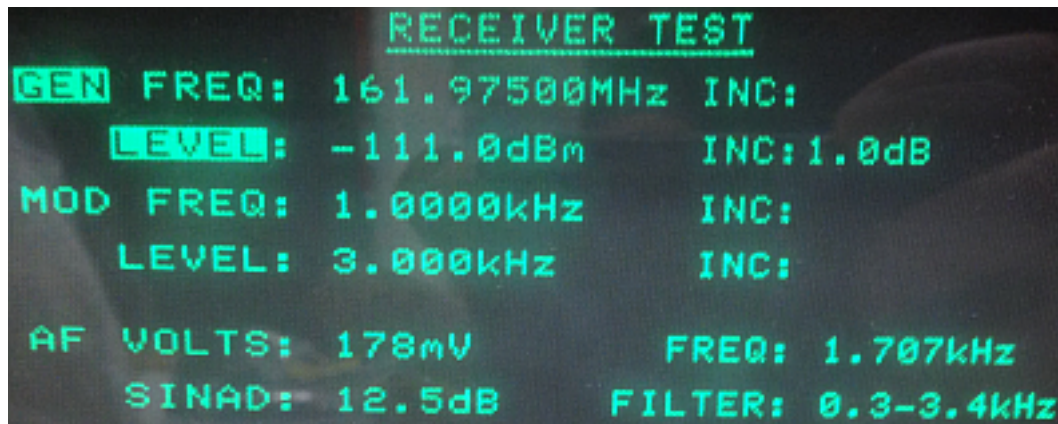


Figure 5.7: The receiver sensitivity test measurements. The signal level of -111dBm produces an audio signal with a SINAD of 12.5dB.

test parameters for SINAD from the display on the 2955B test set. From Figure 5.7 we can see that a signal level of -111dBm at the SDR input maintained a SINAD of 12.5dB, designating the receiver sensitivity level of the SDR. The IEC 62287-1 standard states that the receiver must obtain 20% PER at input signal levels of -107dBm [1]. Repetitive VDM sentences were also observed using Tera Term when an AIS message signal is modulated on the channel with a amplitude of -111dBm. Because the SDR platform achieved a SINAD of 12.5dB at -111dBm it is assumed that it outperforms the IEC 62287-1 receiver sensitivity standard by 4dB. Achieving a higher sensitivity gives the system a marketing edge, as the achievable coverage by a radio system is dictated by its sensitivity.

The sensitivity of the SDR receiver has been observed at -113dBm previously, however the test shown only managed to capture -111dBm. This may have been due to the testing environment and equipment. Further investigation must be done to understand the cause.

Testing receiver performance with a high input level of -7dBm, would result in exceeding the ADC's full scale power, saturating the ADC. Figure 5.8 shows a FFT of the output data from the AD9629. The spurious response of saturating the ADC is very evident in the Nyquist bandwidth, as result of clipping the input waveform. However, the FM demodulated signal still successfully recovers the message signal. This is due to the nature of the FM modulated carrier signal. Because the message signal is represented by the changes in frequency, the demodulator is not concerned with the change in amplitude, therefore it can still produce the modulated signal, even when the peaks of the input waveform have been clipped. One must be cautious

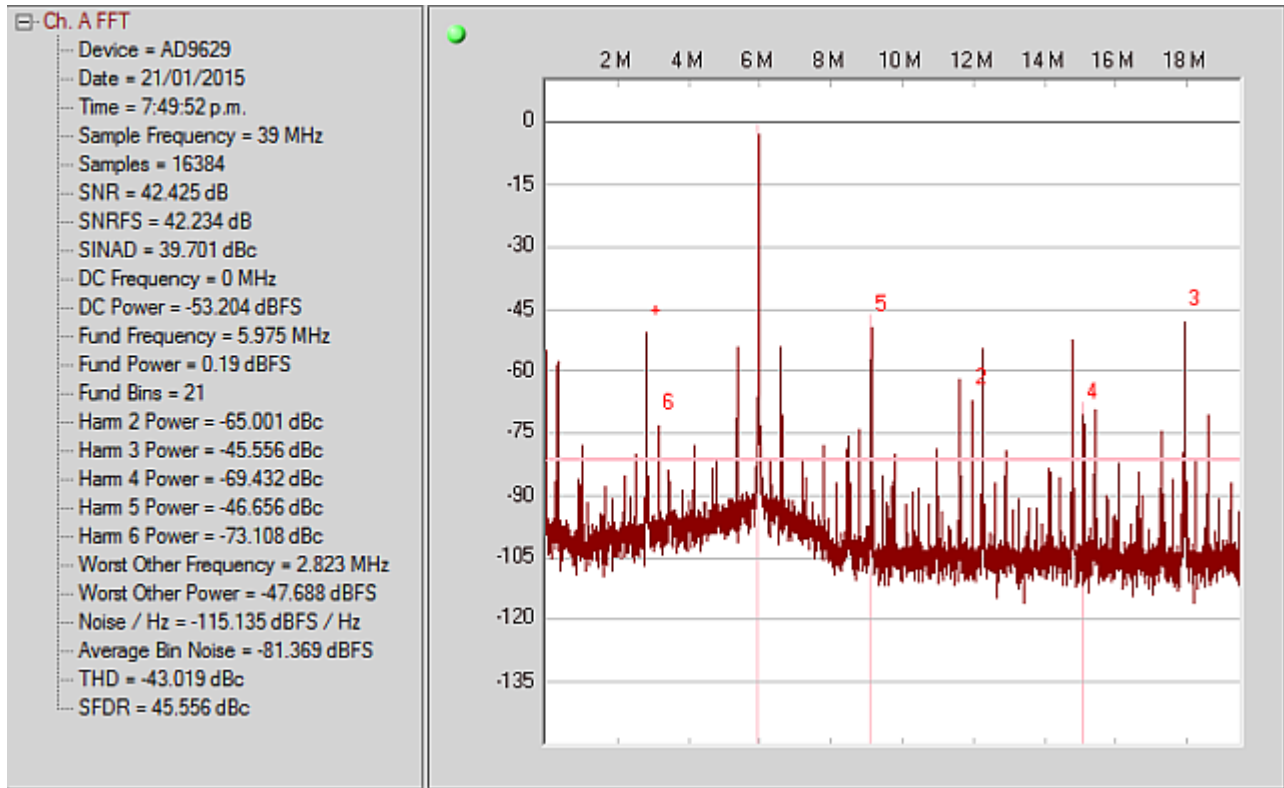


Figure 5.8: A FFT of the output data from the AD9629. This plot shows that the ADC has been saturated by the input signal at -7dBm.

when the ADC saturates, as shown in Figure 5.8 the spurious response can be detrimental to other weak channels within the digitized bandwidth. This is the reason why an AGC is included in the AFE prototype board. Investigation into ADC saturation and AGC implementation is a future recommendation for the development of the SDR design.

The co-channel rejection test simulates a situation where the an unwanted channel is being transmitted on the same frequency as the wanted channel. For this test the unwanted signal is also located on AIS channel one, with a signal level of -111dBm. The wanted signal at -101dBm accomplishes a SINAD of >12dB, successfully outputting the message signal. The VDM sentence was also consistently recovered through Tera Term.

Wideband digitization of the VHF maritime signals highly relies the ADC's dynamic range. The SDR is designed to receive a multitude of signals within the maritime bandwidth. As discussed in Section 3.1.2, the effect of strong adjacent channels in the presence of wanted weak signals is a situation where the 12-bit ADC performance may suffer. The selectivity of the receiver is determined by the adjacent channel sensitivity. This test applies a -31dBm unwanted

signal, frequency modulated with a 400Hz sine wave giving a deviation of $\pm 3\text{kHz}$, at $+25\text{kHz}$ from the wanted signal. The signal level of the wanted signal is -101dBm . This means the ADC must acquire a dynamic range of 70dBc between the two signals to successfully digitize the wanted signal. The SINAD test results showed that the demodulated output did not achieve the SINAD criteria under these conditions. To investigate the achievable dynamic range between the wanted signal and the adjacent channel, the amplitude of the wanted signal was increased until the SINAD reached 12dB . The demodulated message signal obtains a SINAD of 12dB at a signal level of -85dBm , corresponding to a dynamic range of 54dBc . Figure 5.9 illustrates the FFT of the AD9629 output. The unwanted signal located at 5.998MHz nearly over powers the wanted signal at 5.975MHz . It is assumed that the noise about the 5.988MHz signal is due to the phase noise accumulated by the signal generators and the 39MHz LO at the ADC's inputs.

The HP8920A used as the unwanted channel has a phase noise of $<-110\text{dBc/Hz}$ at 1GHz with 20kHz offset. To rule out the possibility of the phase noise from the signal generator, a Rohde and Schwarz signal generator was introduced, providing a cleaner signal source with a rated

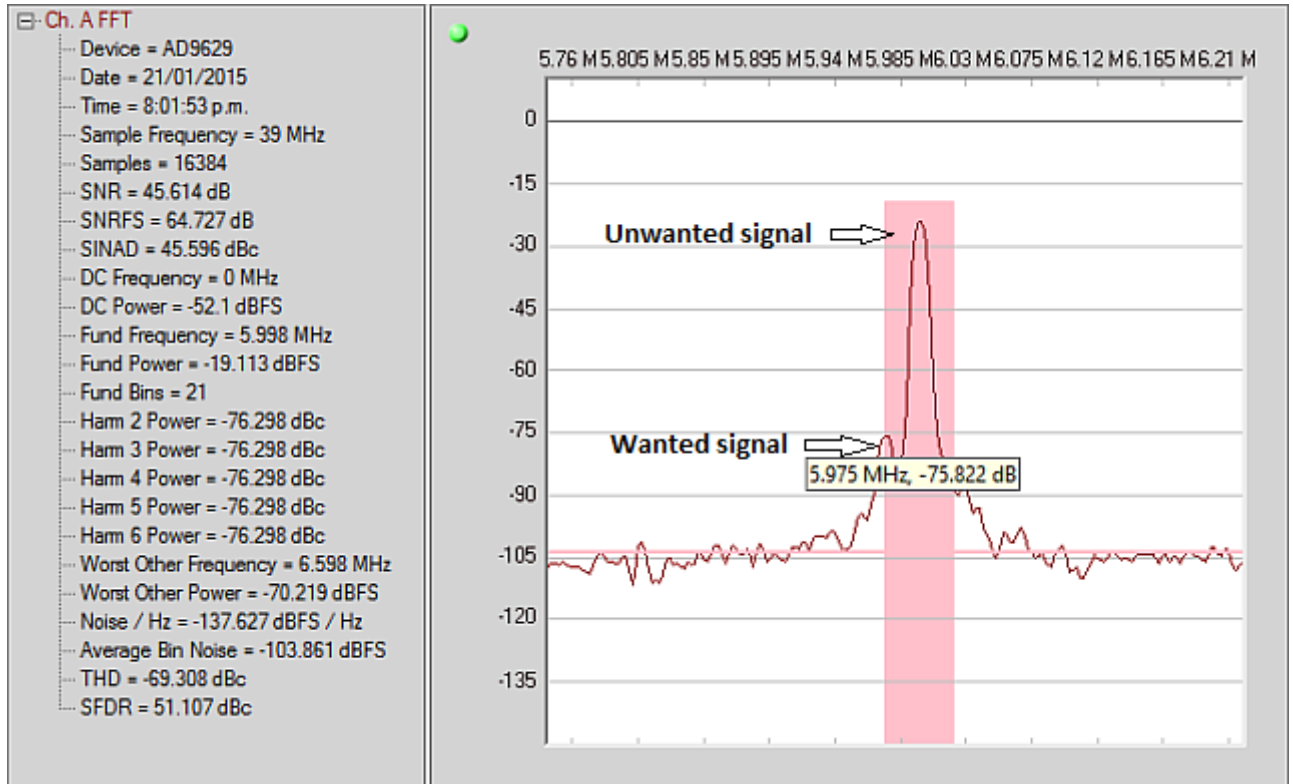


Figure 5.9: FFT of the adjacent channel sensitivity test. The -31dBm unwanted signal is $+25\text{kHz}$ from the -85dBm wanted signal, achieving a dynamic range of 54dBc .

phase noise of $<-122\text{dBc/Hz}$ at 1GHz with 20kHz offset [100]. Applying the unwanted signal using the Rohde and Schwarz to the adjacent channel test still results in the a dynamic range of 54dBc . Therefore, it is assumed that the phase noise of the 39MHz LO is the main cause of the phase noise seen at the ADC output. The RXO2520P LO has a rated jitter of 2ps . This amount of instability to sample a 161.975MHz signal is likely to be the cause of the phase noise observed at the ADC output.

The final test conducted is receiver blocker performance. Good blocking performance is particularly important in scenarios where various radios are in close proximity. When a strong unwanted channel appears at the input it is often found that the sensitivity of the receiver is reduced. This effect is due to the front-end amplifiers going into compression because of the high level blocker [98]. The blocking test will consist of two methods, the first applies a -15dBm blocker signal at -5MHz from the wanted signal, and the second applies -23dBm blocker at -0.5MHz from the wanted signal. Figure 5.10 displays the wanted signal in the presence of an unwanted signal at -5MHz from the wanted signal. By observation the wanted signal in the FFT

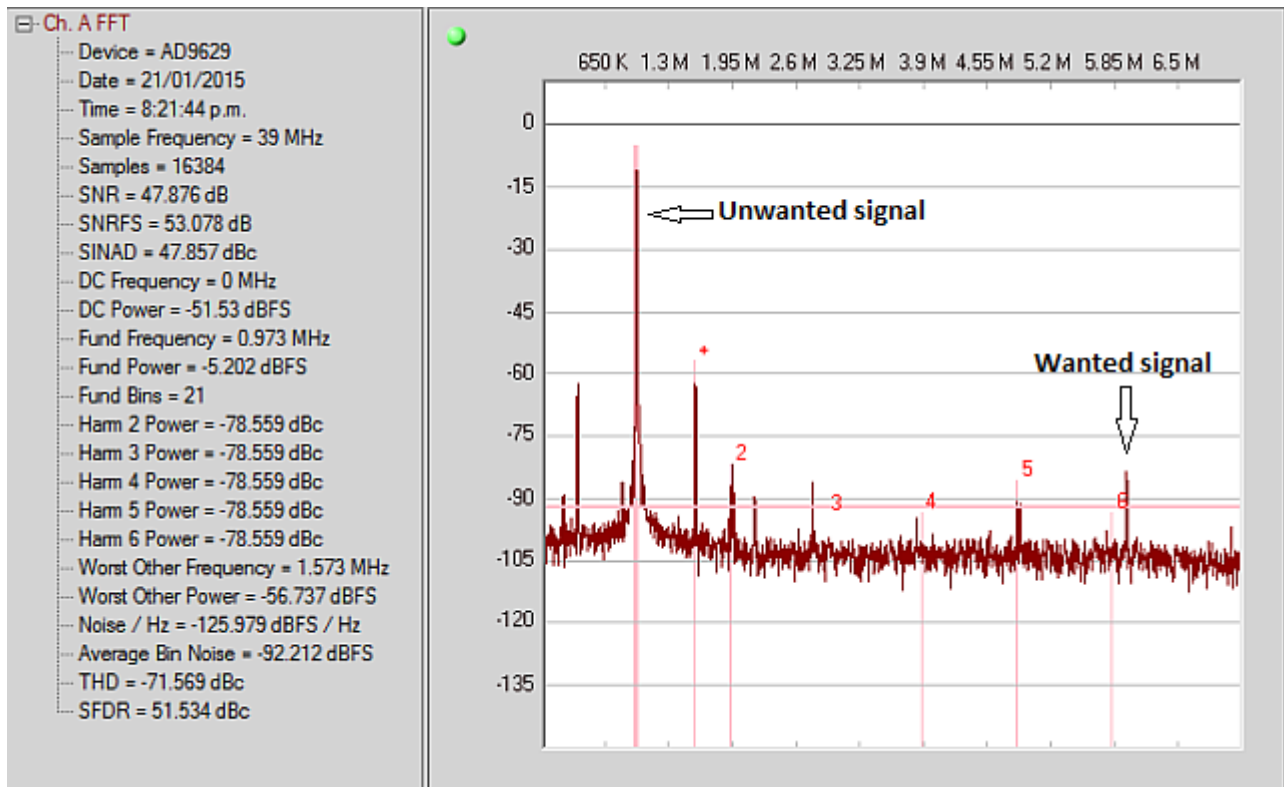


Figure 5.10: A FFT of the blocker test with a unwanted signal at -5MHz from the wanted signal.

is clearly above the noise floor, and further enough away from the frequency component of the blocker to be retained. The audio signal at the codec's output is measured with a SINAD of $>12\text{dB}$. Therefore, the SDR is capable of recovering AIS information under these conditions. Figure 5.11 shows the second blocker test with the unwanted signal -0.5MHz from the wanted signal. The harmonics at $\pm 600\text{MHz}$ about the blocker signal come close to the wanted signal. However, the processing through the DDC removes the unwanted out-of-band frequencies to conserve the AIS channel. The audio signal was also recovered, with SINAD $>12\text{dB}$.

Each test conducted simulated a scenario that is commonly experienced in real collision avoidance applications. The test conditions used were taken from the IEC 62287-1 receiver test methods [1]. Therefore, the results from this chapter display the type of examination a commercial AIS unit will come under.

The test conducted on the SDR platform displayed very promising results. The objective of these tests were to examine the direct digitization receiver using subsampling, and compare its

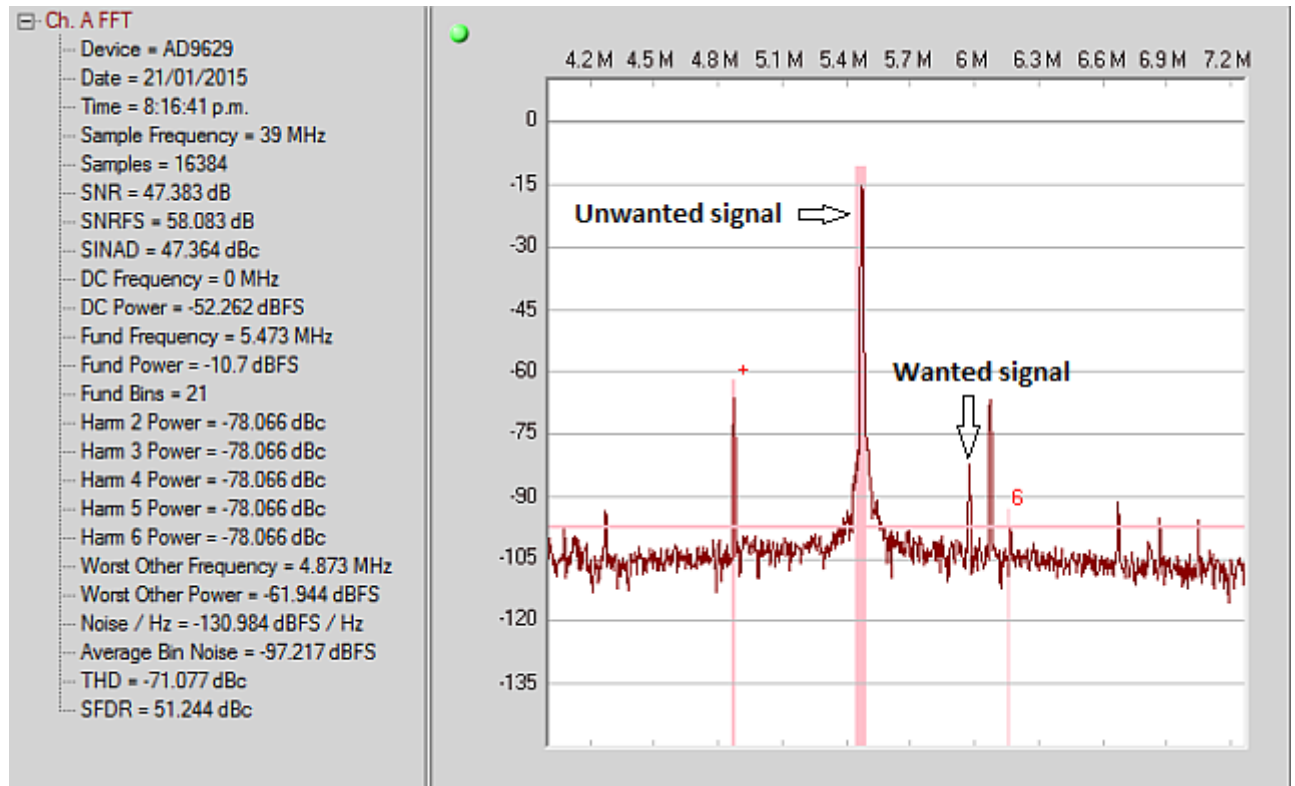


Figure 5.11: A FFT of the blocker test with a unwanted signal at -0.5MHz from the wanted signal.

performance with tests similar to that conducted in the IEC 62287-1 standard. The analysis provided confidence in the receiver design that has been developed. Further optimization must be done to the SDR prototype to maintain the -113dBm sensitivity previously accomplished. Moreover, the concerning characteristics in the SDR's receiver performance is the selectivity displayed in the adjacent channel test. The phase noise on the adjacent channel over powered the wanted signal in Figure 5.9. It is assumed that 39MHz LO used is the cause of this. Investigation into a stable clock must be done in further developments.

The Mimosa board's great selectivity and sensitivity is due to it's superheterodyne architecture. The Mimosa board is capable of -113dBm receiver sensitivity. The objective of the SDR platform is to match the Mimosa's receiver performance. However, further investigation into adjacent channel sensitivity must be done to optimize the current dynamic range of 54dBc.

5.3 COST COMPARISON

As discussed in Section 1.2, the SDR design aims to lower the cost of the existing BOM used for the Mimosa board. The total part count for the receiver path on the Mimosa is 418, including the CMX7032. The total cost amounts to \$106 (NZD). As a result of using direct digitization the SDR reduces the total part count to 111. However, the cost of using an ADC, FPGA and a DSP compensate for the reduction in the parts used. The total cost of the SDR receiver path is \$89. This includes the Cyclone IV EP4CE6 (\$16.26 (NZD) [92]) and the BF526 (\$14.68(NZD) [94]). Therefore, a total of \$17 can be saved in the BOM by achieving a SDR for AIS applications. The direct digitization receiver path dramatically lowers the components used, which will reduce board space and hardware complexity. Moreover, the SDR platform has the capability to access more spectrum, and has the flexibility to apply modifications to the receiver structure via software. Further optimization is also possible within the use of the BF526 DSP, selection of a lower cost DSP may be possible after a full evaluation of AIS baseband processing is completed.

5.4 SUMMARY

This chapter presented the final implementation of the designs developed in Chapter 3 and Chapter 4. It was shown that the SDR is capable of FM demodulating the AIS channel to recover the AIS audio information, this was displayed in Figure 5.4a. The SDR also displayed

the capability of using a second channel (at 157MHz using the second signal generator). A 1kHz tone was FM demodulated from the second channel whilst simultaneously processing AIS channel one, as shown in Figure 5.4. To analyse the quality of voice over FM radio, a portable radio was used to broadcast speech modulated on the 157MHz carrier, this also demonstrating great performance from the dual channels implemented in the SDR.

The AIS audio signal shown in Figure 5.4a was used to feed the CMX7032 to complete the receiver signal chain. This provided the NMEA formatted data that is represented as a VDM sentence. Using a terminal emulator known as Tera Term, the VDM sentences were displayed via PC, as was shown in Figure 5.5. The observation of the VDM packets using Tera Term provided a visual of the packets recovered and the packets lost during each testing phase.

The SDR was examined using test scenarios described in the IEC 62287-1 receiver standards [1]. Under these test conditions the SDR structure shown in Figure 5.6 was used to analyse receiver performance. It was found in Figure 5.7 that the SDR accomplished a receiver sensitivity of -111dBm to obtain a SINAD of 12.5dB. Performing with a sensitivity 4dB higher than the required specification in Table 2.1. The receiver sensitivity has also been observed at levels of -113dBm, maintaining this level must be looked into. The SDR also performed well under high input levels, co-located channels, and blocker conditions. However, the concerning test measure conducted was the adjacent channel sensitivity. AIS channel one in the presences of an unwanted signal at +25kHz from the carrier, only achieved a dynamic range of 54dB. The IEC 62287-1 standard requires a dynamic range of 70dBm between the wanted and unwanted signal. Figure 5.9 showed that the cause is related to the phase noise about the unwanted signal, which over powers the wanted signal when applying the test conditions. It is believed that the phase noise seen in Figure 5.9 is due to the jitter on 39MHz LO used as the clock source for the ADC.

The results conclude that the SDR platform shows a lot of promise, but there are many aspects of the SDR that must be optimised. In Figure 5.8, the AD9629 was under saturation at high input levels, the spurious response showed that any other channels in the VHF maritime band, particularly weak signals, may be lost due to clipping the input waveform. Investigation into the AGC configuration must be completed in future work. Another occurrence that can be detrimental to maritime channels are the harmonics at $\pm 600\text{kHz}$ that appear about the carrier, this was shown in Figure 5.10. Any channels that reside in the presences of these harmonic

may be lost. It is believe that there is some intermodulation occurring at the ADC, further exploration must be conducted.

The cost comparison showed that the SDR receiver path was \$17 (NZD) cheaper than the Mimosa's. This assumes that the CMX7032 function can be encapsulated into the BF526 DSP. Moreover, the total component count was significantly reduced, meaning that the board space required for the SDR is reduced and the complexity of the hardware design is minimised. Overall, the SDR prototype has presented features that are very attractive to incorporate into AIS products. The prototype platform is not far from achieving the IEC 62287-1 receiver standards. It is believed that the required alterations to solve the issues discussed above are very achievable. The results achieved from the SDR prototype provides a lot of motivation to continue with this study.

Chapter 6

CONCLUSION

Reliance on the CMX7032 IC has posed a potential risk on the existing AIS design for the legacy Mimosa board. Component obsolescences of single source IC's, such as the CMX7032 is commonly occurring because of the rapid growth in technology. This has motivated the research into a SDR platform to reduce the dependency on hardware life span. The approach of this project is to implement a software-based system that encapsulates as much signal processing in the digital domain as possible. This method affords software driven flexibility in the design of the radio system.

Use of SDR techniques that directly sample the RF signal through the use of subsampling has been demonstrated. The beauty of this method is that it performs the analog-to-digital conversion without an analog IF stage, shifting the analog processing stages into the digital domain, and reducing the component count throughout the front-end receiver path. Chapter 3 detailed a frequency planning strategy that was developed to purposefully alias the maritime bandwidth into the 19.5MHz Nyquist bandwidth. In Figure 3.6, a sample rate of 39MHz was applied to alias an exact replica of AIS channel one to 5.975MHz, effectively down-converting the AIS signal to a digital IF stage. The frequency planning strategy also benefits from oversampling the AIS signal, this reduces the PSD of the quantization noise within the Nyquist bandwidth. Through the post-processing stages, digital filtering and decimation can produce added process gain to the receiver's SNR. It is calculated that a process gain of 29dB can be obtained by oversampling the channel bandwidth of 26kHz with a 39MHz sample rate.

Executing digital signal processing software on the digitized data at 39MHz required the processing power of an FPGA. Because this project is also driven by cost, the FPGA is dedicated to performing the digital down converter (DDC) functions, performing channelization and sample

rate conversion. Chapter 4 detailed the design of the DDC structure in the FPGA, capable of producing the AIS signal in its I and Q components, at a decimated rate of 52kHz. Figure 4.10 showed the FPGA resources required to implement the DDC for two channels. It was found that the smallest FPGA in the Cyclone IV family (the EPC4E6) is suitable for the SDR platform, costing \$16.25 (NZD) [92].

The decimated sample rate reduced the processing load, allowing a DSP to perform the baseband processing. This gave the BF526 7,692 MACs to encapsulate all the necessary signal processing functions to recover the AIS information. Partitioning the process load between the FPGA and DSP not only reduces costs, but also provides a more software effective platform. As discussed in Section 4.2, the DSP executes the FM demodulation. For future developments, the DSP also has the capability to encapsulate the AIS baseband processing, shifting the CMX7032 functions into the DSP. The complete digital signal chain from RF to an audio signal was implemented with the DE0-Nano (FPGA) board and the BF526 (DSP) evaluation board. VDM sentences are recovered by the CMX7032 to display the AIS information. This proved that the SDR receiver is capable of recovering AIS data from other vessels through the designed receiver processes.

Chapter 5 described test methods and presented results comparing the new receiver performance to the IEC 62287-1 receiver requirements. It was shown that the SDR platform is capable of accomplishing the required sensitivity levels for AIS applications by attaining a 12dB SINAD. The SDR achieves -111dBm sensitivity, outperforming the required level of -107dBm. A sensitivity of -113dBm has also been observed, motivating continued SDR developments. Applying the adjacent channel sensitivity test showed the importance of clean signal sources to reduce noise. Evidence of phase noise about the unwanted adjacent channel was detected, which overpowers the wanted channel. As a result, the dynamic range between the wanted and unwanted channel was only 54dBc, under-performing against the specifications.

Cost comparison between the SDR and the Mimosa receiver paths showed that a total of \$17 (NZD) can be saved by implemented the receiver on a SDR platform. The total component count on the Mimosa board is 418, implementing the traditional superheterodyne receiver architecture. This is indicative of the high volume of components required to complete the analog signal chain. Comparing this is due to the direct digitization method in the SDR, the component count

was found to be reduced to 111. Therefore, the SDR requires less board space, minimises the hardware complexity and results in lower cost.

The SDR methods developed provide a promising solution for Vesper's AIS products. It has been shown that the SDR designed has the potential to provide hardware sustainability as ADCs, FPGA and DSP will continue to grow for the foreseeable future. The software-based solution described is a method that cuts down costs, reduce PCB size and affords reconfigurability through software. The sensitivity capability of the SDR can match the performance of the Mimosa. However, the selectivity of the SDR requires further development. As will be discussed in Figure 6.1, the outstanding issue does not cease the progression of the SDR prototype toward a commercial product. The advantages of SDR presented show that there are benefits worth pursuing. With the rapid growth of high speed technology, cost and performance of ADC, FPGA and DSP devices will continue to improve, making SDR technology an exciting research field.

6.1 FUTURE WORK

An essential step for the SDR platform is compliance with all the receiver performance requirements in IEC 62287-1 [1]. The adjacent channel sensitivity test displayed how critical it is to use a stable signal source. In Figure 5.9, the phase noise on the carrier signal seemed to overpower the wanted signal. By replacing the current 39MHz LO (RXO2520) with a more stable clock source, the phase noise about the unwanted signal should reduce, and improve the dynamic range between adjacent channels. Another method to improve the ADC's dynamic range is to use a higher resolution ADC. However, as discussed in Section 3.1.2, going to a 14 or 16-bit ADC would increase costs significantly.

Saturating the ADC with a high signal level input showed that the SDR can still recover the AIS information. However, saturating the ADC can be detrimental to other digitized signals within the Nyquist bandwidth. The effect of the spurious response in the Nyquist bandwidth was shown in Figure 5.8, illustrating how other maritime channels could potentially be lost when the ADC becomes saturated. Evaluation of the AGC configuration must be analysed so that the SDR can manage the signal levels into the ADC.

Reanalysis of the $\pm 600\text{kHz}$ harmonics about the digitized carrier signal must be completed. A study into intermodulation to identify the cause of these harmonics may provide an indication for

solving this issue. In Section 3.3.2, the structure of the amplifier and filters stages of the analog front-end (AFE prototype) was designed. Calculations showed that the AFE configuration results in a system noise figure of $NF_{sys}=7\text{dB}$. Ideally, the front-end will accomplish a NF_{sys} closer to 3dB, to achieve an efficient receiver design. Re-evaluation of the analog stages must be completed to optimize the system noise figure.

To implement the full evaluation of the SDR for AIS applications, AIS baseband processing must be implemented in the DSP. The process is accomplished digitally by the CMX7032. Therefore, the signal processing functions of the CMX7032 should be able to be executed in the DSP. Research into the algorithms to produce the NMEA formatted data will have to be accomplished. Completing this will provide the final stage for the SDR receiver. Throughout the development of the prototype, results have established the feasibility of the SDR approach for AIS, further development of this prototype is expected to continue at the conclusion of this study.

Appendix A

FM DEMODULATION CODE

```
#include "BF526_system.h"

void Process_Data(void)
{
    // Multiple [1,0,-1,0] and [0,-1,0,1] sequences to obtain I and Q components at base band.
    // Note that multiplying by 0's is not required for more efficiency
    for(i=0; i<Number_of_Samples; i++){
        Q_conv[i] = (iTxBuffer1[i])*-1;
        i++;
        L_conv[i] = (iTxBuffer1[i])*-1;
        i++;
        Q_conv[i] = (iTxBuffer1[i])*1;
        i++;
        L_conv[i] = (iTxBuffer1[i])*1;
    }

    // Low-pass FIR filters implemented for both I and Q components. Note cut-off frequency is
    at 8kHz.

    fir_fr16(L_conv, L_filt, Number_of_Samples, &state);
    fir_fr16(Q_conv, Q_filt, Number_of_Samples, &state);
}
```

// Calculate the magnitude of the message signal by taking the sum of squares. This is used as the denominator of the FM demodulation algorithm.

```
for(i=1; i<Number_of_Samples; i++){
    IQ_magn[i] = (I_filt[i]^2) + (Q_filt[i]^2);
}
```

// Differentiate the I and Q components

```
for(i=0; i<Number_of_Samples-1; i++){
    I_diff[i] = I_filt[i+1] - I_filt[i];
    Q_diff[i] = Q_filt[i+1] - Q_filt[i];
}
```

// FM demodulation algorithm using the filtered and differentiated I and Q components

```
for(i=0; i<Number_of_Samples-1; i++){
    FM_demod[i] = ((I_filt[i+1]*Q_diff[i]) - (Q_filt[i+1]*I_diff[i]))/IQ_magn[i];
}
}
```

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